International Symposium on Low Power Electronics and Design

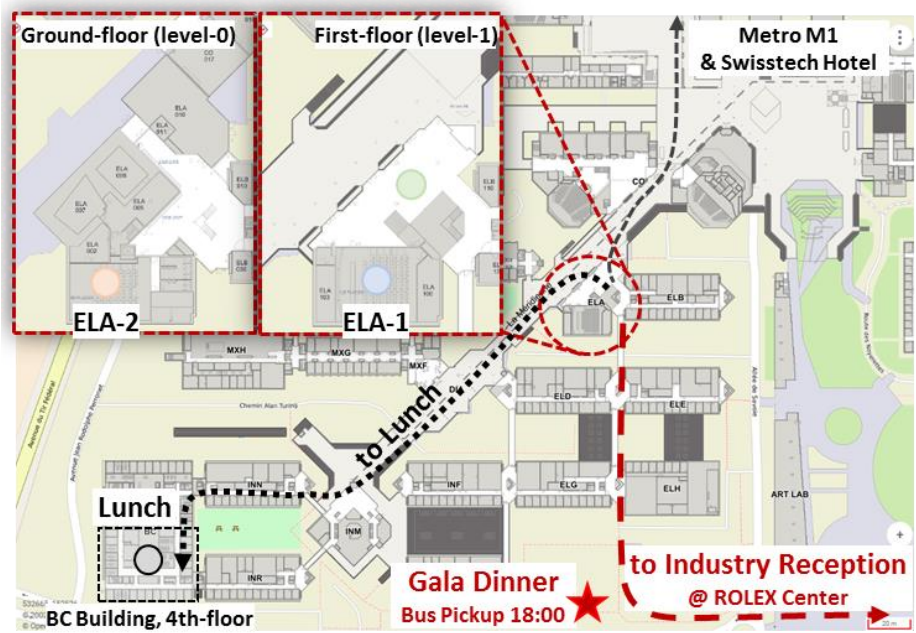
ISLPED 2019

July 29-31, 2019

EPFL, Lausanne, Switzerland

Practicalities

Conference Venue (EPFL) Overview Map



Keynote lectures: ELA-1 Regular Sessions: ELA-1 & ELA-2
Coffee Breaks/Posters: ELA Hallway Lunches: BC Building, 4th floor

Industry Reception & Demos (Monday 18:00 at EPFL ROLEX Center)

The design contest will start with a session of short pitches in ELA-1 and the demos as well as the posters of the industry perspective papers will be shown during the industry reception in the ROLEX Learning Center at EPFL.

Gala Dinner (Tuesday 18:30 at Olympic Museum, bus at EPFL @ 18:00)

The Gala Dinner takes place at the Olympic Museum in Lausanne (Ouchy). The event includes a visit to the museum, an apero, and the dinner. **Busses leave at EPFL (see map for pickup point) at 18:00**. **Return to the hotel is by yourself** with Metro M2 and M1 for hotels at EPFL (bring your metro card). Note: Please be sure to **bring your Dinner Ticket(s).**

WIFI Access at EPFL

Use EDUROAM or connect to SSID **freewifi-epfl** and register and authenticate with your browser by requesting any web page.

Program Overview

ROOM:	*ELA-1*	*ELA-2*
Day-1: Monday, July 29th		
08:00 – 08:30	**Conference Registration**	
08:30 – 09:00	**Welcome by General and Program Co-Chairs**	
09:00 – 10:00	**Keynote Talk 1: Hsien-Hsin Sean Lee, AI Facebook "The Computing Frontiers of Social Network"**	
10:00 – 10:30	**Coffee Break**	
10:30 – 11:45	**Low Power Analog Sensing**	**Power Delivery: Generate, Regulate, Infiltrate**
12:00 – 13:30	**LUNCH (BC-Cafeteria)**	
13:30 – 14:45	**Clocking and Communication Techniques**	**Low-Power Architectures and Frameworks for ML**
14:45 – 15:15	**Coffee Break**	
15:15 – 16:30	**Low Power On-Chip and Chip-To-Chip Communication**	**Artificial Intelligence in System Design**
16:30 – 17:45	**Design Contest Short Pitches**	
18:00 – 20:00	**Industry Reception (Design Contest Demos & Industry Posters)**	
Day-2: Tuesday, July 30th		
9:00 – 10:00	**Keynote Talk 2: Prof. Luca Benini, ETH Zurich "Extreme Edge AI - The Parallel Ultra-low Power (PULP) Approach"**	
10:00 – 10:30	**Coffee Break**	
10:30 – 11:45	**Machine Learning Circuits and Memory Design**	**Low-Power Edge Computing Systems**
12:00 – 13:30	**LUNCH (BC-Cafeteria)**	
13:30 – 14:45	**Approximation for High Energy and Computational Efficiency**	**Energy-Efficient Software for Mobile Applications**
14:45 – 15:15	**Coffee Break**	
15:15 – 16:30	**Memory Efficiency Improvement**	**Special Session In-Memory Computing**
18:30 – 22:00	**Gala Dinner @ Olympic Museum & Awards Bus leaves 18:00 at EPFL**	
Day-3: Wednesday, July 31st		
9:00 – 10:00	**Keynote Talk 3: Prof. Giovanni De Micheli, EPFL "Nanosystems: Technology and Tools"**	
10:00 – 11:00	**Coffee Break**	
11:00 – 12:15	**Application-Centric Optimization of Emerging Technologies**	**Optimization Methodologies for Unconventional Digital Designs**
12:30 – 14:00	**LUNCH (BC-Cafeteria)**	

Monday

9:00 – 10:00 Keynote-1
The Computing Frontiers of Social Network
Hsien-Hsin Sean Lee, *AI Facebook*

Session 1.1/1.2.A: Low Power Analog Sensing

10:30 – 10:55 **A Pulse-Width Modulated Cochlear Implant Interface Electronics with 513 µW Power Consumption**
Halil Andac Yigit, Hasan Ulusan, Muhammed Berat Yuksel, Salar Chamanian, Berkay Çiftci, Aziz Koyuncuoglu, Ali Muhtaroglu and Haluk Kulah

10:55 – 11:20 **A Sound Activity Detector Embedded Low-Power MEMS Microphone Readout Interface for Speech Recognition**
Youngtae Yang, Junsoo Cho, byunggyu lee and Suhwan Kim

11:20 – 11:45 **A Compact Self-Capacitance Sensing Analog Front-End for a Touch Detection in Low Power Mode**
Jiheon Park, Young-Ha Hwang, Jonghyun Oh, Yoonho Song, Jun-Eun Park and Deog-Kyoon Jeong

Session 2.1.A: Power Delivery: Generate, Regulate, Infiltrate

10:30 – 10:55 **A Design Framework for Thermal-Aware Power Delivery Network in 3D MPSoCs with Integrated Flow Cell Arrays**
Halima Najibi, Alexandre Levisse and Marina Zapater

10:55 – 11:20 **Automatic GDSII Generator for On-Chip Voltage Regulator for Easy Integration in Digital SoCs**
Venkata Chaitanya Krishna Chekuri, Nihar Dasari, Arvind Singh and Saibal Mukhopadhyay

11:20 – 11:45 **Power Delivery Resonant Virus: Concept and Application**
Tianhao Shen, Di Gao, Yiyu Shi and Cheng Zhuo

Session 1.1/1.2.B: Clocking and Communication Techniques

13:30 – 13:55 **A Low-Energy Inductive Transceiver using Spike-Latency Encoding for Wireless 3D Integration**
Benjamin Fletcher, Shidhartha Das and Terrence Mak

13:55 – 14:20 **A Low-Power and Low-Noise 20:1 Serializer with Two Calibration Loops in 55-nm CMOS**
Yong-Un Jeong, Joo-Hyung Chae, Sung-Phil Choi, Jaekwang Yun, Shinhyun Jeong and Suhwan Kim

14:20 – 14:45 **Robust Low Power Clock Synchronization for Multi-Die Systems**
Ragh Kuttappa, Baris Taskin, Scott Lerner, Vasil Pano and Ioannis Savidis

Monday

Session 2.2.A: Low-Power Architectures and Frameworks for ML

13:30 – 13:55 **An Automated Approximation Methodology for Arithmetic Circuits**
Sayandip De, Jos Huisken and Henk Corporaal

13:55 – 14:20 **An Ultra-Efficient Memristor-Based DNN Framework with Structured Pruning and Quantization Using ADMM**
Geng Yuan, Xiaolong Ma, Caiwen Ding, Sheng Lin, Tianyun Zhang, Zeinab S. Jalali, Yilong Zhao, Li Jiang, Sucheta Soundarajan, Yanzhi Wang

14:20 – 14:45 **DYSPINDLE : DYNAMIC SPIKE BUNDLING FOR ENERGY-EFFICIENT SPIKING NEURAL NETWORKS**
Sarada Krithivasan, Sanchari Sen, Swagath Venkataramani and Anand Raghunathan

Session 1.3.A: Low Power On-Chip and Chip-To-Chip Communication

15:15 – 15:40 **On Trade-off Between Static and Dynamic Power Consumption in NoC Power Gating**
Di Zhu, Yunfan Li and Lizhong Chen

15:40 – 16:05 **Muffin: Minimally-Buffered Zero-Delay Power-Gating Technique in On-Chip Routers**
Hossein Farrokhbakht, Hadi Mardani Kamali and Natalie Enright Jerger

16:05 – 16:30 **Concurrent Multipoint-to-Multipoint Communication on Interposer Channels**
Lejie Lu, Richard Afoakwa, Michael Huang and Hui Wu

Session 2.3.A: Artificial Intelligence in System Design

15:15 – 15:40 **TEA-DNN: the Quest for Time-Energy-Accuracy Co-optimized Deep Neural Networks**
Lile Cai, Anne-Maelle Barneche, Arthur Herbout, Chuan Sheng Foo, Jie Lin, Vijay Ramaseshan Chandrasekhar and Mohamed M. Sabry

15:40 – 16:05 **CNN-based Camera-less User Attention Detection for Smartphone Power Management**
Daniele Jahier Pagliari, Matteo Ansaldi, Enrico Macii, Massimo Poncino

16:05 – 16:30 **MemGANs: Memory Management for Energy-Efficient Acceleration of Complex Computations in Hardware Architectures for Generative Adversarial Networks**
Muhammad Abdullah Hanif, Muhammad Zuhaib Akbar, Rehan Ahmed, Semeen Rehman, Axel Jantsch, Muhammad Shafique

Monday

Industry Perspective Posters (Presented during Industry Reception)

1	**Comparative evaluation of Body Biasing and Voltage Scaling for Low-Power Design on 28nm UTBB FD-SOI Technology** Ricardo Gomez Gomez, Edwige Bano and Sylvain Clerc
2	**Enhanced 3D Implementation of an Arm Cortex-A Microprocessor** Xiaoqing Xu, Mudit Bhargava, Steve Moore, Saurabh Sinha and Brian Cline

Design Contest Demos (Pitch Session and Industry Reception)

Processor Innovations

1	**Exceeding Pessimistic Margins on ARMv8 Servers for Energy Efficient Processing in Edge/Cloud** G. Papadimitriou, A. Chatzidimitriou, D. Gizopoulos, P. Nikolaou, Z. Hadjilambrou, Y. Sazeides, L. Mukhanov, K. Tovletoglou, G. Karakonstantis and D. Guilhot
2	**Energy-Quality Scalable Monocular Depth Estimation for Embedded Systems** A. Cipolletta, V. Peluso, A. Calimera, E. Macii, M. Poggi, F. Tosi and S. Mattoccia
3	**Implementation of Software Defined Energy Management for Xilinx Zynq UltraScale+ MPSoC** V. Zivojnovic, D. Mista and N. Katic
4	**A 50MHz Low Power SoC Operating on a 0.48V Supply at 25°C** K. Han, S. Lee, J.-J. Lee, W. Lee and M. Pedram
5	**Design and Validation of A Two-Phase Gravity-Driven Micro-Scale Thermosyphon** A. Iranfar, A. Seuret, I. Penas, J. B. Marcinichen, M. Zapater, J. Thome and D. Atienza
6	**Realizing Energy-Efficient Dependable Systems with Variably-Reliable DRAMs** K. Tovletoglou, L. Mukhanov and G. Karakonstantis
7	**An 88fJ / 40 MHz [0.4V] – 0.61pJ / 1GHz [0.9V] Dual Mode Logic 8x8-bit Multiplier Accumulator with a Self-Adjustment Mechanism in FD-SOI** I. Stanger, N. Shavit, R. Taco and A. Fish

Machine Learning

8	**Efficient Model Compression and Hardware-Aware Quantization for Object Detection on FPGAs** M. Sun, G. Yuan, N. Liu, K. Xu, X. Lin, and Y. Wang
9	**Thinker-IM: An Energy-Efficient Speech Recognition Processor with Computing-in-Memory SRAM and Predictive Execution** R. Guo, Y. Liu, S. Zheng, S.-Y- Wu, P. Ouyang, W.-S. Khwa, C. Xi, J.-J. Chen, X. Li, L. Liu, M.-F. Chang, S. Wei and S. Yin

Monday

10	**Vau da Muntanialas: Towards Real-Time Speech Recognition on an Energy-Efficient Systolic Array of LSTM Accelerators** G. Paulin, L. Cavigelli, F. Conti and L. Benini
11	**Neuromorphic System for Temporal Data Classification** H. Fang, A. Shrestha, D. Rider and Q. Qiu
12	**An Embedded Deep Learning Accelerator for Intelligent Microcontroller Units** F. Su, J. Yue, H. Tian and Y. Liu
13	**STICKER: An energy efficient sparse-aware neural network processor** Z. Yuan, Y. Yang, H. Tian, T. Wu, H. Yang and Y. Liu

Edge Devices

14	**FLASH: Content-based Power-saving Design for Scrolling Operations in Browser Applications on Mobile OLED Devices** H.-C. Chang, Y.-C. Yang, L.-Y. Yu and C.-H. Lin
15	**Always-On VGA Vision Sensor with Pixel-Wise Double-Threshold Background Rejection for Event-Detection** Y. Zou, M. Gottardi, M. Lecca and M. Perenzoni
16	**e-Glass for Real-Time Brain Activity Monitoring in the Internet of Things (IoT) Era** R. Zanetti, D. Sopic, A. Aminifar and D. Atienza
17	**Self-Sustainable Embedded High-Precision and Low Latency UWB Localization** P. Mayer, C. Schnetzler, M. Magno and L. Benini
18	**2.45-GHz Wireless Power Transfer for BLE-connected Smart Motion Detection Sensor** R. Dekimpe, P. Xu, M. Schramme, N. Janatian, I. Stupia, M. Drouguet, P. Gérard, C. Craeye, L. Vandendorpe, D. Flandre and D. Bol
19	**PULP-DroNet: Open Source and Open Hardware Artificial Intelligence for Fully Autonomous Navigation on Nano-UAVs** D. Palossi, F. Conti, D. Rossi and L. Benini
20	**InfiniWolf: A Self-Sustaining and Energy Efficient Multi-Sensor SmartWatch** X. Wang, M. Magno, D. Baret, L. Schulthess, M. Eggimann and L. Benini
21	**SecureTouch: A Zero-Power Reciever For Body Communication and Secure Applications** P. Mayer, F. Villani, K. Weber and M. Magno

Tuesday

9:00 – 10:00 Keynote-2
Extreme Edge AI–The Parallel Ultra-low Power (PULP) Approach
Luca Benini, *ETH Zurich*

Session 1.1/1.2.C: Machine Learning Circuits and Memory Design

10:30 – 10:55 **K-Nearest Neighbor Hardware Accelerator Using In-Memory Computing SRAM**
Jyotishman Saikia, Shihui Yin, Zhewei Jiang, Mingoo Seok and Jae-sun Seo

10:55 – 11:20 **A Logic Compatible 4T Dual Embedded DRAM Array for In-Memory Computation of Deep Neural Networks**
Taegeun Yoo, Hyunjoon Kim, Qian Chen, Tony Tae-Hyoung Kim and Bongjin Kim

11:20 – 11:45 **A 65nm switched source line sub-threshold ROM using data encoding, with 0.3V Vmin and 47fJ/b access energy**
Supreet Jeloka, Pranay Prabhat, Graham Knight and James Myers

Session 2.2.B: Low-power Edge Computing Systems

10:30 – 10:55 **Autonomous I/O for Intermittent IoT Systems**
Yu-Chen Lin, Pi-Cheng Hsiu and Tei-Wei Kuo

10:55 – 11:20 **BottleNet: A Deep Learning Architecture for Intelligent Mobile Cloud Computing Services**
Amir Erfan Eshratifar, Amirhossein Esmaili and Massoud Pedram

11:20 – 11:45 **Similarity-Based LSTM Architecture for Energy-Efficient Edge-Level Speech Recognition**
Junseo Joe, Jaeha Kung, Sunggu Lee and Youngjoo Lee

Session 1.3.B: Approximation for High Energy and Computational Efficiency

13:30 – 13:55 **MixNet: An Energy-Scalable and Computationally Lightweight Deep Learning Accelerator**
Sangwoo Jung, Seungsik Moon, Youngjoo Lee and Jaeha Kung

13:55 – 14:20 **A^2M: Approximate Algebraic Memory Using Polynomial Rings**
Dong Kai Wang and Nam Sung Kim

14:20 – 14:45 **Compressing Sparse Ternary Weight Convolutional Neural Networks for Efficient Hardware Acceleration**
Hyeonwook Wi, Hyeonuk Kim, Seungkyu Choi and Lee-sup Kim

Tuesday

Session 2.3.B: Energy-Efficient Software for Mobile Applications

13:30 – 13:55 **FLASH: Content-based Power-saving Design for Scrolling Operations in Browser Applications on Mobile OLED Devices**
Hao-Chun Chang, Yu-Chieh Yang, Liang-Yan Yu and Chun-Han Lin

13:55 – 14:20 **Balancing Memory Accesses for Energy-Efficient Graph Analytics Accelerators**
Mingyu Yan, Xing Hu, Shuangchen Li, Itir Akgun, Han Li, Xin Ma, Lei Deng, Xiaochun Ye, Zhimin Zhang, Dongrui Fan and Yuan Xie

14:20 – 14:45 **Rethinking Last-level-cache Write-back Strategy for MLC STT-RAM Main Memory with Asymmetric Write Energy**
Yu-Pei Liang, Tseng-Yi Chen, Yuan-Hao Chang, Shuo-Han Chen, Pei-Yu Chen and Wei-Kuan Shih

Session 1.3.C: Memory Efficiency Improvement

15:15 – 15:40 **Improving Energy Efficiency by Memoizing Data Access Information**
Michael Stokes, Ryan Baird, Zhaoxiang Jin, David Whalley and Soner Onder

15:40 – 16:05 **Exploring the Relation between Monolithic 3D L1 GPU Cache Capacity and Warp Scheduling Efficiency**
Cong Thuan Do, Young-Ho Gong, Cheol Hong Kim, Seon Wook Kim and Sung Woo Chung

16:05 – 16:30 **SHRIMP: Efficient Instruction Delivery with Domain Wall Memory**
Joonas Multanen, Asif Ali Khan, Pekka Jääskeläinen, Fazal Hameed and Jeronimo Castrillon

Special Session: In-Memory Computing

15:15 – 15:40 **Unified Memory-Computing Architecture with Memristive Devices**
Qing Wu

15:40 – 16:05 **Phase-change memory enables energy-efficient brain-inspired computing**
Manuel Le Gallo

16:05 – 16:30 **Slashing energy and runtime with BLADE, an in-cache computing architecture for edge devices**
Alexandre Levisse

Wednesday

9:00 – 10:00 Keynote-3
Nanosystems: Technology and Tools
Giovanni De Micheli, *EPFL*

10:00 – 11:00 Poster Session

1	**3DTUBE: A DESIGN FRAMEWORK FOR HIGH-VARIATION CARBON NANOTUBE-BASED TRANSISTOR TECHNOLOGY** Aporva Amarnath, Javad Bagherzadeh, Jielun Tan and Ron Dreslinski
2	**A PROBABILISTIC APPROACH TO ENERGY-CONSTRAINED MIXED-CRITICALITY SYSTEMS** F. Reghenzani, G. Massari and W. Fornaciari
3	**ADDRESSING TEMPORAL VARIATIONS IN QUBIT QUALITY METRICS FOR PARAMETERIZED QUANTUM CIRCUITS** M. ALAM, A. Ash- Saki and S. Ghosh
4	**AN ENERGY EFFICIENT ON-CHIP LEARNING ARCHITECTURE FOR STDP BASED SPARSE CODING** H. Kim, H. Tang and J. Park
5	**BATTERY-AWARE ELECTRIC TRUCK DELIVERY ROUTE PLANNER** D. Baek, Y. Chen, N. Chang, E. Macii, M. Poncino
6	**COMPHD: EFFICIENT HYPERDIMENSIONAL COMPUTING USING MODEL COMPRESSION** J. Morris, M. Imani, S. Bosch, A. Thomas, H. Shu and T. Rosing
7	**FPGA-based Acceleration of Binary Neural Network Training with Minimized Off-Chip Memory Access** P. K. Chundi, P. Liu, S. Park, S. Lee and M. Seok
8	**ENERGY-AUTONOMOUS MCU OPERATING IN SUB-VT REGIME WITH TIGHTLY-INTEGRATED ENERGY-HARVESTER** J. Deng, J.-L. Nagel, L. Zahnd, M. Pons, D. Ruffieux, C. Arm, P. Persechini and S. Emery
9	**LOCAL LEARNING IN RRAM NEURAL NETWORKS WITH SPARSE DIRECT FEEDBACK ALIGNMENT** B. Crafton, P. Basnet, M. West, E. Vogel and A. Raychowdhury
10	**MESSAGEFUSION: ON-PATH MESSAGE COALESCING FOR ENERGY EFFICIENT AND SCALABLE GRAPH ANALYTICS** L. Belayneh, A. Addisie and V. Bertacco
11	**MODELING AND OPTIMIZATION OF CHIP COOLING WITH TWO-PHASE VAPOR CHAMBERS** Z. Yuan, G. Vaartstra, P. Shukla, S. Reda, E. Wang and A. Coskun

12 **NON-VOLATILE MEMORY UTILIZING RECONFIGURABLE FERROELECTRIC TRANSISTORS TO ENABLE DIFFERENTIAL READ AND ENERGY-EFFICIENT IN-MEMORY COMPUTATION.**
S. K. Thirumala, S. Jain, A. Raghunathan and S. Gupta

13 **SECO: A SCALABLE ACCURACY APPROXIMATE EXPONENTIAL FUNCTION VIA CROSS-LAYER OPTIMIZATION**
D. Wu, T. Chen, C.-F. Chen, O. Ahia, J. San Miguel, M. Lipasti and Y. Kim

14 **SHINE: A NOVEL SHA-3 IMPLEMENTATION USING RERAM-BASED IN-MEMORY COMPUTING**
K. Nagarajan, S. S. Ensan, M. N. I. Khan, S. Ghosh and A. Chattopadhyay

15 **TEMPERATURE-AWARE ADAPTIVE VM ALLOCATION IN HETEROGENEOUS DATA CENTERS**
Y. G. Kim, J. I. Kim, S. H. Choi, S. Y. Kim and S. W. Chung

16 **TIP: A TEMPERATURE EFFECT INVERSION-AWARE ULTRA-LOW POWER SYSTEM-ON-CHIP PLATFORM**
K. Han, S. Lee, J.-J. Lee, W. Lee and M. Pedram

Session 1.3/2.3.D: Application-Centric Optimization of Emerging Technologies

11:00 – 11:25 **RAPID: A ReRAM Processing in Memory Architecture for DNA Sequence Alignment**
Saransh Gupta, Mohsen Imani, Behnam Khaleghi, Venkatesh Kumar and Tajana Rosing

11:25 – 11:50 **HR3AM: a Heat Resilient design for RRAM based neuromorphic computing**
Xiao Liu, Minxuan Zhou, Tajana Rosing and JISHEN ZHAO

11:50 – 12:15 **NCFET-Aware Voltage Scaling**
Sami Salamin, Martin Rapp, Hussam Amrouch, Girish Pahwa, Yogesh Chauhan and Joerg Henkel

Session 2.1/2.2/2.3: Optimization Methodologies for Unconventional Digital System Designs

11:00 – 11:25 **Towards a Complete Methodology for Synthesizing Bundled-Data Asynchronous Circuits on FPGAs**
Kshitij Bhardwaj, Paolo Mantovani, Luca Carloni and Steven M. Nowick

11:25 – 11:50 **Tier Partitioning and Flip-flop Relocation Methods for Clock Trees in Monolithic 3D ICs**
Da Eun Shim, Sai Surya Kiran Pentapati, Jeehyun Lee and Sung Kyu Lim

11:50 – 12:15 **VCAM: Variation Compensation through Activation Matching for Analog Binarized Neural Networks**
Jaehyun Kim, Chaeun Lee, Jihun Kim, Yumin Kim, Cheol Seong Hwang and Kiyoung Choi

Organizing Committee

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