CASES 2016


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Call for Papers

International Conference on Compilers, Architectures and Synthesis For Embedded Systems

CASES is a forum where researchers, developers and practitioners exchange information on the latest advances in compilers and architectures for high performance embedded systems. In addition to our core areas of technical interest including embedded system architectures, compilers and embedded systems software, memory architectures, architectures targeting power, reliability and security, and emerging application domains, we especially encourage papers that address architectural synthesis and compiler techniques for heterogeneous and accelerator-rich architectures.

Abstract submission:
April 1, 2016

Full paper submission:
April 8, 2016 (Firm deadline)

Conference:
October 2-7, 2016

Venue:
Pittsburgh Marriott City Center

Previously unpublished papers containing significant novel ideas and technical results are solicited in the following areas:

Embedded Architectures: GPU and accelerator architectures, Reconfigurable processors, FPGAs and extensible cores System-on-chip (SoC) architectures, Multi-core and many-core processors for embedded computing, On-chip communication architectures and networks-on-chip, 3D architectures, integration and synthesis and Embedded system design space exploration & methodology

Compilers and Embedded Systems Software: Compilation for reliability, power, performance, Static and dynamic execution time analysis, Specification of embedded systems, Compiler support for GPUs, FPGAs and heterogeneous systems

Memory: Memory system architecture and management, Non-volatile and other emerging memory technologies, Scratchpad, smart caches and compiler controlled memories

Power, Reliability and Security: Secure architectures and hardware security, Modeling & online management of reliability, power, performance, Validation, verification & debugging of embedded software

Emerging Application Domains: Architectures/compilers for Internet of Things (IoT) platforms, Architectures/compilers for wearables and other small form factor devices, Cyber-physical systems architectures, Architectures for emerging nanoscale devices, Programmable microfluidics, Accelerators for data analytics and learning, Neuromorphic and cognitive computing

Paper Process: This year ESWeek will introduce a two-stage review process in order to further increase quality. Papers passing the first stage need to revise their work within a short time frame of around two weeks. Further details will be published at least two months before the submission deadline. As always, all accepted papers come with a talk and a poster presentation. Each accepted paper requires one full conference registration.

ESWeek General Chairs:
Jörg Henkel, KIT Karlsruhe, DE
Lothar Thiele, ETH Zürich, CH

CASES Program Chairs:
Siddharth Garg, New York University, US
Laura Pozzi, University of Lugano, CH

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