CODES+ISSS 2016

Call for Papers

International Conference on Hardware/Software Codesign and System Synthesis
October 2-7, Pittsburgh, USA

The International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) is the premier event in system-level design, modeling, analysis, and implementation of modern embedded and cyber-physical systems, from system-level specification and optimization down to system synthesis of multi-processor hardware/software implementations. The conference is a forum bringing together academic research and industrial practice for all aspects related to system-level and hardware/software co-design. CODES+ISSS 2016 is part of the Embedded Systems Week (ESWeek) 2016.

CODES+ISSS Program Chairs:
Andreas Gerstlauer, The University of Texas at Austin, US
Andy Pimentel, University of Amsterdam, NL

Abstract submission:
April 1, 2016
Full paper submission:
April 8, 2016 (Firm deadline)
First paper notification:
May 20, 2016
Revised paper submission:
June 10, 2016
Notification of acceptance:
July 1, 2016
Camera-ready version:
July 15, 2016

CODES+ISSS invites contributions on specification, modelling, design, analysis, and implementation of embedded and cyber-physical systems. The following relevant areas are representative but not exhaustive. We welcome submissions on novel solutions, new challenges, and emerging technologies in all these areas:

Track 1) System-level design – Specification, modelling, refinement, system synthesis, partitioning, hardware-software co-design, design space exploration, hybrid system modelling and design, and model-based design.

Track 2) Domain and application-specific design- Analysis, design, and optimization techniques for multimedia, medical, automotive, cyber-physical, and other specialized application domains.

Track 3) Embedded software - Language and library support, compilers, runtimes, parallelization, software verification, memory management, virtual machines, operating systems, real-time support, and middleware.

Track 4) Embedded systems architecture - Architecture and micro-architecture design, exploration and optimization including application-specific processors, reconfigurable architectures, storage, memory and communication systems, and networks-on-chip.

Track 5) Large-scale, adaptive systems - Many-cores, heterogeneous systems, data centers, cloud computing, networked and distributed systems, sensor networks, and design for adaptivity and reconfigurability.

Track 6) Simulation, validation and verification - Hardware/software co-simulation, verification and validation methodologies, formal verification, hardware-accelerated simulation, simulation and verification languages, models and benchmarks.

Track 7) Power-aware systems - Power- and energy-aware system design and methodologies ranging from low-power embedded and cyber-physical systems to energy-efficient large scale systems such as Green IT and Smart Grid.

Track 8) Security and reliability – Cross-layer reliability, resilience and fault tolerance, test methodology, design for testability, hardware and software security, and cyber-physical system security.

Track 9) Industrial practices and case studies - Practical impact on current and/or future industries, application of state-of-the-art methodologies and tools in various application areas including wireless, networking, multimedia, automotive, cyber-physical, medical systems, etc.

Submission Process: This year ESWeek will introduce a two-stage review process in order to further increase quality. Full submission details are available at http://www.esweek.org/author-information. All accepted papers come with a talk and a poster presentation. Each accepted paper requires one full ESWeek conference registration.

http://www.esweek.org/codes/about