EMBEDDED SYSTEMS WEEK

13TH ACM/IEEE EMBEDDED SYSTEMS WEEK

2017 ESWEEK PROGRAM

OCTOBER 15-20, 2017 | SEOUL | SOUTH KOREA

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WELCOME TO ESWEEK 2017

Lothar Thiele | General Chair
Swiss Federal Institute of Technology, Zurich, Switzerland

Soonhoi Ha | Vice-General Chair
Seoul National Univ., Korea

Welcome to ESWEEK 2017 in Seoul!

Embedded Systems Week (ESWEEK) is the premier event covering all aspects of embedded systems and software. By bringing together three leading conferences (CASES, CODES+ISSS, EMSOFT), a special IoT day, three symposia (ESTIMedia, RSP, NOCS), and hot-topic workshops and tutorials, ESWEEK presents attendees a wide range of topics unveiling state of the art embedded systems design and HW/SW architectures.

For the first time, ESWEEK 2017 will implement a journal-integrated publication model for the conferences CASES, CODES+ISSS, and EMSOFT, where all journal-track papers will be published in the ACM Transactions on Embedded Computing Systems. To this end, the review process of the conferences was conducted in two stages with the opportunity of minor/major revisions before the final decision. Acceptance rates have been about 25% for all conferences with a total number of 289 submissions to the journal track. In addition, 37 Work-in-Progress track papers have been selected and will be published in the ESWEEK Proceedings.

The technical program on Monday, Tuesday, and Wednesday consists of 5 special sessions and 28 regular sessions from the three conferences. There is a strong emphasis on interaction as at the end of each session there is a poster presentation during which all presented papers can be discussed with the authors.

Like last year, we will make Tuesday a special IoT day, focusing on the newest developments in the "Internet of Things" (IoT) from an embedded systems point of view. A sequence of three sessions is exclusively devoted to this subject with contributions from all of the three conferences.

Highlights of the ESWEEK program are three distinguished keynote talks by the most prominent leaders in academia and industry, covering most relevant trends for future embedded systems and providing deep insights into technology drivers. Kurt Keutzer from the Univ. of California, Berkeley, covers efficient implementations of deep neural networks: "Small Neural Nets Are Beautiful: Enabling Embedded Systems with Small Deep-Neural-Network Architectures." Feng Zhao, Chief Technology Officer and Vice President for Advanced R&D from Haier, will be the keynote speaker at the IoT day with "IoT from the Lab to the Real World." Finally, the Wednesday keynote by Gernot Heiser from the Univ. of New South Wales, Australia, will emphasize the importance and challenges related to the trustworthiness of embedded systems, i.e., security, safety and dependability: "Trustworthy Operating Systems for Critical Embedded and Cyberphysical Systems."

The tutorials on Sunday precede the conferences and are an excellent opportunity to get in-depth knowledge in new trends and hot topics. There are six tutorials covering a wide scope, from embedded neural networks and approximate computing via heterogeneous and real-time architectures up to energy harvesting in the Internet of Things.

Thursday and Friday are the days for the symposia and workshops. Besides the two long-term members of ESWEEK, ESTIMedia (Embedded Systems for Real-Time Multimedia) and RSP (Rapid System Prototyping), we are proud that the successful International Symposium on Networks on CHIP (NOCS) also joins ESWEEK 2017. The workshops cover a wide range of important topics in embedded systems such as Declarative Embedded and Cyber-Physical Systems (DECPS), Design, Modeling and Evaluation of Cyber-Physical Systems (CyPhy), Embedded and Cyber-Physical Systems Education (WESE), and Highly Efficient Neural Networks Design (HENND).

The conference program will conclude with the traditional panel on Wednesday afternoon focusing on "Machine Learning for Embedded Systems: Hype or Lasting Impact?" Top experts from academia and industry will share their views on this controversial topic.

The organization of ESWEEK was only possible with the continuous support and help from many volunteers: The program chairs with their program committee members, the organizers of workshops, tutorials and symposia, all members of the organization committee, and last but not least, the local arrangements chairs and their team. Our special thank goes to the head of the steering committee, Nikil Dutt, the past chair, Joerg Henkel and the publication chair, Linh Thi Xuan Phan. They have been the driving forces in the implementation of the new journal-integrated publication model of ESWEEK.

We are looking forward to meeting you at the inspiring and interesting ESWEEK 2017 in Seoul!

GENERAL INFORMATION

Welcome to Seoul

Seoul is the capital of Korea with over 600 years of history. It is the heart of Korea's culture and education as well as politics and economics.

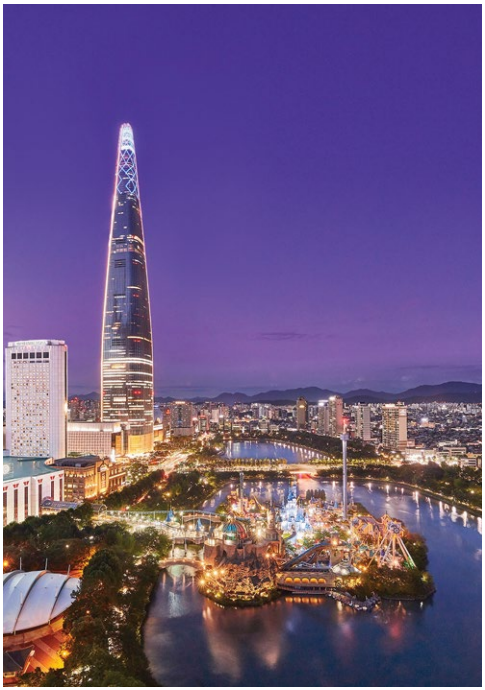
In Seoul, the world's 10th largest city, the past and present co-exist in a fascinating way. Ancient palaces, gates, gardens, and valuable art collections in museums attest to the illustrious past of the city while the glistening facades of soaring skyscrapers and the busy streets represent its vibrant present. Seoul is home to many old historic sites like the Gyeongbokgung and Changdeokgung Palaces, and places with traditional culture like Bukchon Hanok Village, Insa-dong, and Namdaemun Market. The shopping and entertainment districts of Myeong-dong and Apgujeong, and Asia's largest underground shopping center Coex Mall also draw a large number of tourists every year. The Hangang River, which runs through the center of the city, is also a distinctive landscape of Seoul that offers a myriad of resting areas for citizens.

Seoul has now turned its attention into becoming an eco-friendly and culturally rich city after the recent decades of development and growth that helped improve life quality. In Seoul, visitors will find highly skilled human resources and the world's best information-technology infrastructure. Seoul's beautiful natural environment, low tax burdens, and social security expenses for foreign business make it a great place to invest, do business, and live.

Conference Registration Fees

Conference registration allows attendance to any of the three ESWEEK conferences, CODES+ISSS, CASES, and EMSOFT. Conference registration includes lunch on conference days, online conference proceedings, the Sunday Welcome Reception, and one ticket to the banquet. Student Conference registration does not include a banquet ticket, but one can be purchased. Workshops, Tutorials, and Symposia can be added on to your registration for an additional fee.

Conference Member	**$850**
Conference Non-Member	**$975**
Conference Student Member	**$450**
Conference Student Non-Member	**$600**
Thursday & Friday Workshops Member/Non-Member	**$350**
Thursday & Friday Workshops Students	**$250**
Tutorial (each tutorial)	**$75**
Symposia	
ESTIMedia Member/Non-Member	**$350**
ESTIMedia Student	**$250**
NOCS Member/Non-Member	**$550**
NOCS Student	**$380**
RSP Member/Non-Member	**$400**
RSP Student	**$300**



ESWEEK 2017 OVERVIEW

Sunday, October 15

Tutorials

Welcome Reception

Monday, October 16

Opening Session

Keynote by Kurt Keutzer

CASES, CODES+ISSS, & EMSOFT Sessions

Poster Sessions

Technical Program Committee Dinner

Tuesday, October 17

Keynote by Feng Zhao

CASES, CODES+ISSS, EMSOFT & IoT Day Sessions

Poster Sessions

Hotel Signiel, Lotte World Tower - Social Event

Wednesday, October 18

Keynote by Gernot Heiser

CASES, CODES+ISSS, EMSOFT & IoT Day Sessions

Poster Sessions

Best Paper Awards Ceremony

ESWEEK Panel

Thursday, October 19

CyPhy'17 Workshop

DECPS'17 Workshop

WESE'17 Workshop

ESTIMedia'17 Symposium

NOCS'17 Symposium

RSP Symposium

Caffe2 Tutorial

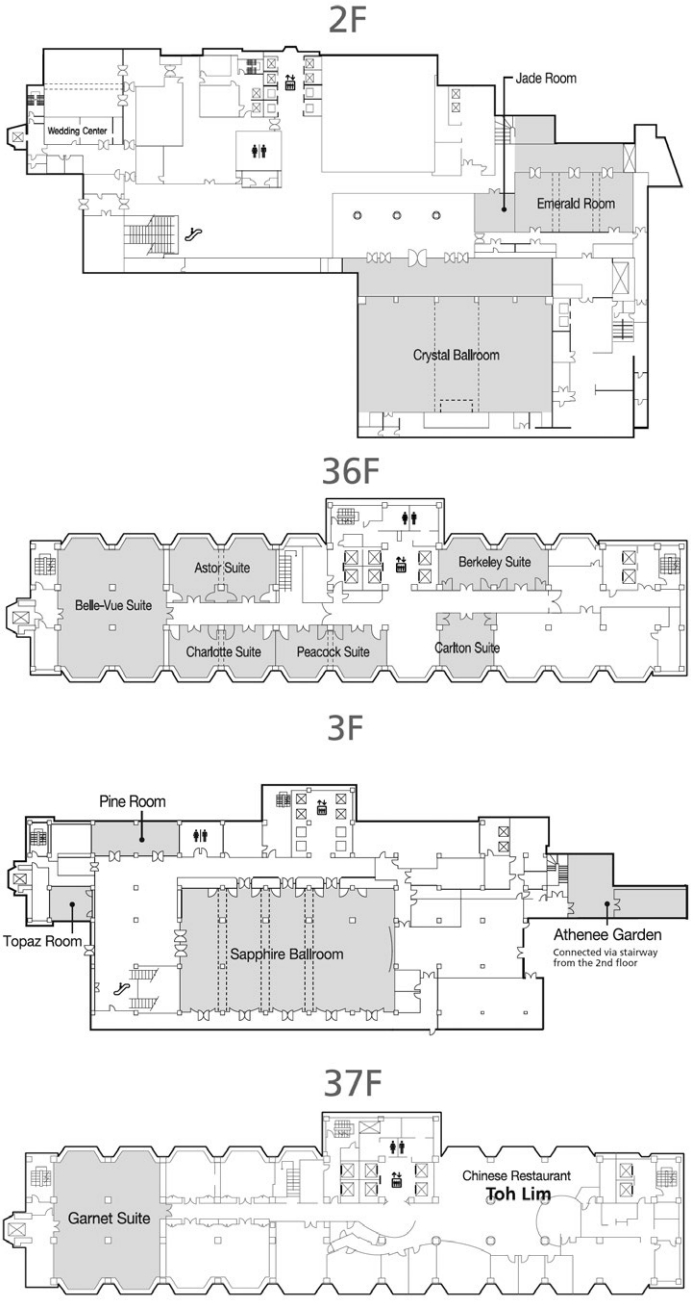
Friday, October 20

HENND'17 Workshop

NOCS'17 Symposium

RSP Symposium

Conference Venue Floorplan



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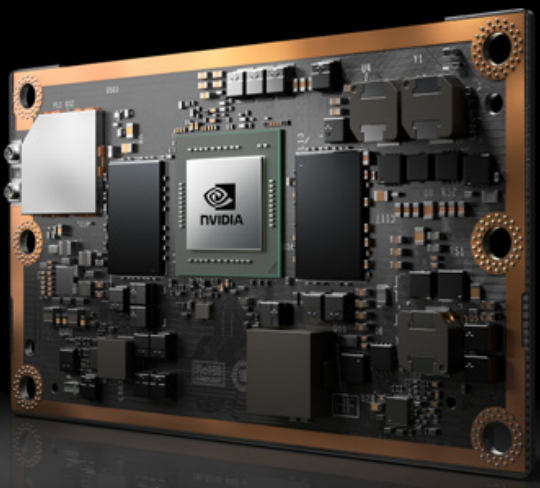

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BEST PAPER CANDIDATES

CASES

MODULAR COMPILATION OF HYBRID SYSTEMS FOR EMULATION AND LARGE SCALE SIMULATION

Authors:

Avinash Malik - *Univ. of Auckland*
Partha Roop - *Univ. of Auckland*
Sidharta Andalam - *Nanyang Technological Univ.*
Mark Trew - *Univ. of Auckland*
Michael Mendler - *Univ. of Bamberg*

AN OUT-OF-ORDER LOAD-STORE QUEUE FOR SPATIAL COMPUTING

Authors:

Lana Josipovic - *École Polytechnique Fédérale de Lausanne*
Philip Brisk - *Univ. of California, Riverside*
Paolo Ienne - *École Polytechnique Fédérale de Lausanne*

LOW-COST MEMORY FAULT TOLERANCE FOR IoT DEVICES

Authors:

Mark Gottscho - *Univ. of California, Los Angeles*
Irina Alam - *Univ. of California, Los Angeles*
Clayton Schoeny - *Univ. of California, Los Angeles*
Lara Dolecek - *Univ. of California, Los Angeles*
Puneet Gupta - *Univ. of California, Los Angeles*

CODES + ISSS

CAMSURE: SECURE CONTENT-ADDRESSABLE MEMORY FOR APPROXIMATE SEARCH

Authors:

M. Sadegh Riazi - *Univ. of California, San Diego*
Mohammad Samragh - *Univ. of California, San Diego*
Farinaz Koushanfar - *Univ. of California, San Diego*

NUCLEUS: FINDING THE SHARING LIMIT OF HETEROGENEOUS CORES

Authors:

Ilias Vougioukas - *Univ. of Southampton*
Andreas Sanberg - *ARM Ltd.*
Stephan Diestelhorst - *ARM Ltd.*
Bashir Al-Hashimi - *Univ. of Southampton*
Geoff Merrett - *Univ. of Southampton*

FLEXIBLE PV-CELL MODELING FOR ENERGY HARVESTING IN WEARABLE IOT APPLICATIONS

Authors:

Jaehyun Park - *Arizona State Univ.*
Hitesh Joshi - *Arizona State Univ.*
Hyung Gyu Lee - *Daegu Univ.*
Sayfe Kiaei - *Arizona State Univ.*
Umit Ogras - *Arizona State Univ.*

EMSOFT

COMPOSITIONAL RELATIONAL ABSTRACTIONS FOR NONLINEAR HYBRID SYSTEMS

Authors:

Xin Chen - *Univ. of Colorado*
Sergio Mover - *Univ. of Colorado*
Sriram Sankaranarayanan - *Univ. of Colorado*

SECURITY-AWARE SCHEDULING OF EMBEDDED CONTROL TASKS

Authors:

Vuk Lesi - *Duke Univ.*
Ilija Jovanov - *Duke Univ.*
Miroslav Pajic - *Duke Univ.*

OPTIMIZATION OF REAL-TIME SOFTWARE IMPLEMENTING MULTI-RATE SYNCHRONOUS FINITE STATE MACHINES

Authors:

Yecheng Zhao - *Virginia Polytechnic Institute and State Univ.*
Chao Peng - *National Univ. of Defense Technology*
Haibo Zeng - *Virginia Polytechnic Institute and State Univ.*
Zonghua Gu - *Zhejiang Univ.*

SUNDAY, OCTOBER 15
TUTORIALS SCHEDULE

	Berkely, 36F	*Charlotte, 36F*	*Peacock, 36F*
08:30 - 12:30	Approximate Computing with Approximate Circuits: Methodologies and Applications	HW/SW Compilation and Synthesis for SoCs	Beyond the Deadline: New Interfaces Between Control and Scheduling for the Design and Analysis of Critical Embedded Systems
10:00 - 10:30	Coffee Break | Room: Belle-vue, 36F		
13:30 - 17:00	Neural Networks on FPGAs and other Embedded Platforms	State of the Art Energy Harvesting for IoT	Designing Multi-Bank Memories for Heterogeneous Architectures
15:00 - 15:30	Coffee Break | Room: Belle-vue, 36F		
18:00 - 20:30	Welcome Reception | Room: Belle-vue, 36F		

Tutorial 1 - Approximate Computing with Approximate Circuits: Methodologies and Applications

Time: 08:30 - 12:30 | Room: Berkely, 36F

Organizers:

Lukas Sekanina - *Brno Univ. of Technology,*
Jie Han - *Univ. of Alberta*

In recent years, approximate computing emerged as a promising approach to the design of energy efficient computer systems, by relaxing the requirement of strict exactness in computation. Approximate computing research spans from devices and circuits, up to architecture and software levels. This tutorial provides a brief overview of approximate computing. It is then focused on circuit approximation. We systematically present the approaches developed for approximation of key arithmetic circuits (such as adders and multipliers) and general-purpose circuit approximation methods. Approximate designs are presented for selected applications ranging from simple image filters to deep neural networks used for image classification. We will also discuss relaxed equivalence checking techniques developed to provide formal guarantees on error bounds.

Biographies:

Lukas Sekanina received all his degrees (Ing. in 1999, Ph.D in 2002) from Brno Univ. of Technology, Czech Republic. He was awarded with the Fulbright scholarship to work with NASA Jet Propulsion Laboratory at Caltech in 2004. He has served as an associate editor of IEEE Transactions on Evolutionary Computation (2011-2014), Genetic Programming and Evolvable Machines Journal and International Journal of Innovative Computing and Applications. He (co) authored over 150 papers mainly on evolutionary design and evolvable hardware and 1 patent. He is currently a full professor and Head of the Department of Computers Systems at Faculty of Information Technology, Brno Univ. of Technology.

Jie Han received the B.Sc. degree in electronic engineering from Tsinghua Univ., Beijing, China, in 1999 and the Ph.D. degree from Delft Univ. of Technology, The Netherlands, in 2004. He is currently an associate professor in the Department of Electrical and Computer Engineering at the Univ. of Alberta, Edmonton, AB, Canada. He is serving as an associate editor for IEEE Transactions on Emerging Topics in Computing (TETC). He served as a General Chair for GLSVLSI 2017 and DFT 2013, and a Technical Program Chair for GLSVLSI 2016 and DFT 2012. He has published more than 100 technical papers.

Speakers:

Lukas Sekanina - *Brno Univ. of Technology,*
Jie Han - *Univ. of Alberta*

Tutorial 2 - HW/SW Compilation and Synthesis for SoCs

Time: 08:30 - 12:30 | Room: Charlotte, 36F

Organizer:

Heiko Falk - *Hamburg Univ. of Technology*

Today's Systems-on-Chip (SoCs) must satisfy a multitude of interrelated design constraints, e.g. performance, power/energy efficiency, reliability or real-time capability. Due to these inter-dependencies of constraints, HW/SW co-design of SoCs is a challenging task that involves modelling, optimization, evaluation and design space exploration. This tutorial covers techniques for generating efficient software taking hardware characteristics into account.

The tutorial starts with a review of typical SoC design flows , illustrates the interplay between design constraints and presents synthesis techniques allowing systematic trade-offs. The consideration of multiple design constraints during software compilation will be covered in the second part of the tutorial, with a focus on optimizing energy consumption, quality of service and performance. Hardware-aware compilation and its potential to exploit HW features provided by modern SoC architectures will be demonstrated afterwards. Finally, compilation techniques for parallel, safety-critical systems with real-time constraints will be addressed in the fourth part of the tutorial.

Biographies:

Fadi Kurdahi received his BE in Electrical Engineering from the American Univ. of Beirut in 1981 and the PhD from the Univ. of Southern California in 1987. Since then, he has been a faculty at the Department of Electrical Engineering & Computer Science at Univ. of California, Irvine where he serves as the Associate Dean for Graduate and Professional Studies of the Henry Samueli School of Engineering and the Director of the Center for Embedded & Cyber-physical Systems (CECS). He conducts research in design methodologies of large scale and cyber-physical systems.

Peter Marwedel studied physics at the Univ. of Kiel, Germany. He received a Dr. rer. nat. degree in physics in 1974 and a Dr. Habil. degree in computer science in 1987. Since 1989, he held a chair for computer engineering and embedded systems at the computer science department of TU Dortmund. His research interests include design automation for embedded systems, in particular the generation of efficient embedded and cyber-physical system software.

Aviral Shrivastava is Associate Professor in the School of Computing Informatics and Decisions Systems Engineering at the Arizona State Univ., where he has established and heads the Compiler and Microarchitecture Labs (CML). He received his PhD and Masters from the Univ. of California, Irvine, and bachelors in Computer Science and Engineering from the Indian Institute of Technology, Delhi. His research interests cover compilers and microarchitectures for heterogeneous and many-core computing, protecting computation from soft errors, and precise timing for cyber-physical systems.

Heiko Falk studied computer science at Dortmund Univ., Germany. He received his PhD degree from the same Univ. in 2004 for his work on source code transformation of embedded applications. In 2011, he joined the Institute of Embedded Systems and Real-Time Systems of Ulm Univ. as Associate Professor. Since 2015, he is heading the Institute of Embedded Systems at Hamburg Univ. of Technology. His work covers compilation and optimization for timing predictability, performance and energy efficiency.

Speakers:

Fadi Kurdahi - *Univ. of California, Irvine,*
Peter Marwedel - *Technische Univ. Dortmund,*
Aviral Shrivastava - *Arizona State Univ.,*
Heiko Falk - *Hamburg Univ. of Technology*

Tutorial 3 - Beyond the Deadline: New Interfaces Between Control and Scheduling for the Design and Analysis of Critical Embedded Systems

Time: 08:30 - 12:30 | Room: Peacock, 36F

Organizers:

Rolf Ernst - *Technische Univ. Braunschweig,*
Rafik Henia - *Thales Research and Technology,*
Sophie Quinton - *INRIA*

The objective of this tutorial is to put into perspective the role of deadlines in the design and analysis of critical embedded systems as well as to propose and discuss alternatives.

In current industrial practice, deadlines are used to isolate the control design process from the timing verification process. The control engineer can then work with idealized timing assumptions while the timing architect focuses on establishing that the specified deadline (derived from the sampling period) is always met. This use of deadlines as the interface between control and timing presents several limitations. First, the functional behavior of a system is influenced by timing effects such as sampling jitter even if deadlines are met. Second, and more importantly, requiring all deadlines to be met is an unnecessarily strong requirement.

There is a need for a more efficient approach to the co-design of industrial control applications between control engineering and real-time systems engineering. The purpose of this tutorial is to motivate and present state of the art and recent results in this direction. The invited speakers are academics and practitioners who are recognized experts in control and/or real-time systems design and verification working with new interfaces between these two worlds.

Biographies:

Rolf Ernst received a diploma in computer science and a Dr.-Ing. in electrical engineering from the Univ. of Erlangen-Nuremberg, Germany. He was a Member of Technical Staff in the Computer Aided Design & Test Laboratory at Bell Laboratories, Allentown, PA. Since 1990, he has been a professor of electrical engineering at the Technical Univ. of Braunschweig, Germany, where he chairs a Univ. institute of 50 researchers and staff covering embedded systems research from computer architecture and real-time systems theory to challenging automotive, aerospace, or smart building applications. His research is or was funded by national and European programs as well as by companies, such as BMW, Bosch, Daimler, Ford, GM, Toyota, Volkswagen, Intel, EADS, Siemens, or Thales. He chaired major events, such as ICCAD, DATE or ESWEEK. He is an IEEE Fellow, a DATE Fellow, and served as an ACM-SIGDA Distinguished Lecturer. He is a member of the German National Academy of Science and Engineering, acatech. He received the EDAA Lifetime Achievement Award 2014.

Rafik Henia graduated from the Technical Univ. of Braunschweig (TUBS) in 2003. He worked as a research assistant at the Institute of Computer and Network Engineering at TUBS with research topics related to the timing verification for real-time embedded systems. Since 2009, he has been a Research Engineer at Thales Research and Technology France, Critical Embedded Systems Lab. He works on several R&D projects with Thales avionics, aerospace, telecommunication and defense divisions, whose goals deal with model-based performance design and verification of real-time embedded systems. He was involved in several national and European research projects.

Sophie Quinton is a researcher at Inria Grenoble – Rhône-Alpes in France. She received her Ph.D. degree from the Univ. of Grenoble, in 2011. She was a graduate research assistant at the VERIMAG laboratory and a postdoc in the Embedded System Design Automation group of the Institute of Computer and Network Engineering at TU Braunschweig. Her research focus is mostly on real-time schedulability analysis and contract-based design and verification of systems of components. She has been a PC member of a dozen conferences and workshops and has published in conferences such as CAV, RTSS, DATE, ECRTS, etc.

Marco Di Natale is an IEEE Senior member and Full Professor at the Scuola Superiore Sant'Anna, where he held the position of Director of the ReTiS Lab until 2006. He received his PhD from Scuola Superiore Sant'Anna, he was a visiting Researcher at the Univ. of California, Berkeley in 2006 and 2008, and is currently visiting Fellow for the United Technologies corporation. He's been a researcher in the area of realtime and embedded systems for more than 20 years, being author or co-author of more than 200 scientific papers, winner of six best paper awards and one best presentation award.

Steffen Linsenmayer obtained his M.Sc. degree in Engineering Cybernetics from the Univ. of Stuttgart, Germany. During his Master studies he had an Internship at Robert Bosch GmbH and a stay at KTH, Royal Institute of Technology in Stockholm, Sweden. Since 2015 he is a research and teaching assistant at the Institute for Systems Theory and Automatic

Control and a doctoral student in the Graduate School Simulation Technology at the Univ. of Stuttgart under the supervision of Frank Allgöwer. His main research interests are in the area of Networked Control Systems with a focus on suitable network abstractions.

Dirk Ziegenbein studied Electrical Engineering at Technical Univ. of Braunschweig and Virginia Tech. He received a Ph.D. at Technical Univ. of Braunschweig for his dissertation on modeling and design of embedded systems. In 2002, Dirk Ziegenbein joined Bosch Research and worked on topics such as software component technology and scheduling analysis. From 2007 to 2012, he was responsible for the product management of embedded software engineering tools at ETAS GmbH. Then, Dirk Ziegenbein took over the roles of senior expert for embedded software design and analysis and section manager for software systems engineering at Bosch Research. Dirk Ziegenbein serves in various technical program committees as well as an expert for the European Commission.

Speakers:

Marco di Natale - *Scuola Superiore Sant'Anna*
Steffen Linsenmayer - *Univ. Stuttgart*
Dirk Ziegenbein - *Bosch Research*

Tutorial 4 - Neural Networks on FPGAs and other Embedded Platforms

Time: 13:30 - 17:00 | Room: Berkely, 36F

Organizer:

Nachiket Kapre - *Univ. of Waterloo*

Neural networks are enjoying widespread attention from industry and academia to address problems in different application domains such as vision, speech, and reasoning. The core computational kernels in such networks push modern embedded devices to their limits in terms of their compute capacity, and memory bandwidth and power usage. In this tutorial, we will aim to understand the sources of this complexity in neural network evaluations. We will then focus on implementing the computation across various embedded hardware platforms and identify the opportunities for customizing the mapping. In particular, we will focus on Convolutional Neural Networks, as well as NENGO, a biologically plausible model for brain-scale neural networks with applications to robotics and motion control. We will also take a closer look at the role of FPGAs in supporting efficient evaluation of such networks. This tutorial is aimed at students and practitioners who want to learn about optimizing neural networks on modern embedded platforms.

Biographies:

Nachiket Kapre is an Assistant Professor in the Department of Electrical and Computer Engineering at Univ. of Waterloo, Canada. He was previously an Assistant Professor at Nanyang Technological Univ., Singapore in the School of Computer Engineering (2012-2016) and an Imperial College Junior Research Fellow (2010-2012). He has received his M.S in Electrical Engineering (2005) and Computer Science (2006) and a PhD in Computer Science (2010) from California Institute of Technology, Pasadena. He is primarily interested in understanding and exploiting the potential of parallel, spatial architectures such as FPGAs for energy-efficient computing. His research has won best paper awards at FPT 2010, FPL 2015, and CASES 2016.

Dr. Terrence C. Stewart is a Research Associate with the Centre for Theoretical Neuroscience at the Univ. of Waterloo. He was a primary developer of Spaun, the first large-scale biologically realistic brain simulation capable of performing multiple tasks. His current work is on further developing the neural "compiler" Nengo (which translates high-level algorithms into neurons), and extending it to work with diverse neuromorphic hardware. This includes digital neuromorphic hardware (such as SpiNNaker) and analog neuromorphic hardware (such as Neurogrid). The core emphasis is on identifying and developing algorithms that are efficient on massively parallel hardware.

Professor Guy Lemieux is CEO of VectorBlox Computing Inc. and a Professor in the Department of Electrical and Computer Engineering at The Univ. of British Columbia. He has a research background in FPGA-based computing, FPGA devices, and place and route algorithms for FPGAs. He did his PhD at the Univ. of Toronto, and is a registered Professional Engineer with APEGBC.

Speakers:

Nachiket Kapre - *Univ. of Waterloo,*
Terry Stewart - *Univ. of Waterloo,*
Guy Lemieux - *Univ. of British Columbia*

Tutorial 5 - State of the Art Energy Harvesting for IoT

Time: 13:30 - 17:00 | Room: Charlotte, 36F

Organizers:

Sehwan Kim - *Dankook Univ.,*
Pai H. Chou - *Univ. of California, Irvine*

This tutorial is a half-day collection of four lectures for researchers and practitioners who want to learn about the state of the art in energy harvesting for the Internet of Things (IoT). Tens of billions of connected devices will be deployed in the next decade, but regularly changing the batteries in all these devices will be difficult and expensive. A potential solution is to harvest energy from a variety of environmental sources such as light, temperature gradients, vibration, movement, air flow, or radio signals. Output levels are typically of the order of milliwatts or lower, sufficient for low-power electronic devices that would otherwise be powered by small batteries. Four invited speakers will introduce different aspects of energy harvesting, from energy sources and circuits to systems and applications..

Biographies:

Sehwan Kim is Assistant Professor of Biomedical Engineering at Dankook Univ., South Korea. He received his Ph.D. degree in Electrical Engineering and Computer Science from the Univ. of California, Irvine in 2011. Prior to his Ph.D., he has 8-year industrial experience including Samsung Electronics as a senior engineer for R&D of mobile phones. His research interests include low-power circuits and systems design, IoT-based biomedical systems, and efficient energy harvesting. He is a member of several Technical Program Committee of DAC and ASP-DAC. He won the Low Power Design Contest Award at ISLPED 2013 and Chancellor's Best Teaching Award, Dankook Univ., 2016.

Pai H. Chou received the A.B. degree in computer science from the Univ. of California, Berkeley, in 1990, and the M.S. and Ph.D. degrees in computer science and engineering from the Univ. of Washington, Seattle, in 1993 and 1998, respectively. He is a Professor in the Department of Electrical Engineering and Computer Science, Univ. of California, Irvine; and in computer science at the National Tsing Hua Univ., Hsinchu, Taiwan. His research interests include wireless sensing systems, low-power design, energy harvesting, and system synthesis. Dr. Chou is a recipient of the National Science Foundation CAREER Award.

Aatmesh Shrivastava received his Ph.D. degree from the Univ. of Virginia in 2014. Prior to his Ph.D., he worked as a senior design engineer at Texas Instruments, Bangalore from 2006 to 2010. From 2014 to 2016, he worked at an IoT start-up PsiKick as senior design director. In August 2016, he joined Northeastern Univ., where he is now working as an Assistant Professor in the Electrical Engineering Department. His research interests include self-powered and ultra-low power circuits and system, energy-harvesting and power-first system/computer architecture, internet-of-things, ultra-low power bio-medical and neural circuits, exascale computing, and high-reliability circuits and system design

Daniel Chou is the founder and CEO of Flexwave Co., Ltd., in Hsinchu, Taiwan. He is the inventor of the flexible waveguide photovoltaics, an organic polymer material that can enable energy harvesting of a wide range of IoT devices without taking up extra areas. He was a Ph.D. candidate at National Chiao-Tung Univ. in Electro-optical Engineering from 2011-2014. He was an R&D Engineer at a2peak Power in 2009 and Technical Consultant at Viswell Technology in 2011. He received the scholarship grant of Chung Hua Rotary Educational Foundation in 2012 and was a recipient of Best Paper Award in Optics & Photonics International Conference in 2013.

Davide Brunelli is Associate Professor with the Univ. of Trento, Italy. He received the M.S. (cum laude) and Ph.D. degrees in electrical engineering from the Univ. of Bologna, Italy, in 2002 and 2007, respectively. His current research interests include smart grids and the development of new techniques of energy scavenging for IoT and embedded systems, the optimization of low-power and low-cost consumer electronics, and the interaction and design issues in embedded personal and wearable devices. He is leading the activity on Energy Efficiency in the IEEE Smart City initiative for the city of Trento. He is a senior member of the IEEE.

Speakers:

Aatmesh Shrivastava - *Northeastern Univ.,*
Daniel Chou - *Flexwave Co. Ltd.,*
Davide Brunelli - *Univ. of Trento,*
Sehwan Kim - *Dankook Univ.*

Tutorial 6 - Designing Multi-Bank Memories for Heterogeneous Architectures

Time: 13:30 - 17:00 | Room: Peacock, 36F

Organizers:

Christian Pilato - *Univ. della Svizzera Italiana,*
Luca P. Carloni - *Columbia Univ.*

Modern computing systems feature an increasing number of heterogeneous components, including multiple general-purpose processors and special-purpose accelerators. Local memories are critical for the performance of these components and are often responsible for a large fraction of their area occupation and power dissipation. Consequently, it is important to tailor each of these memories to the specific characteristics of the particular component that is accessing the data it stores.

We present a methodology for the generation of multi-bank memories for heterogeneous architectures that is supported by MNEMOSYNE, an open-source prototype CAD tool. MNEMOSYNE performs various technology-aware optimizations to reduce the memory costs by efficiently reusing the physical banks for storing different types of data. We illustrate our methodology by showing how it can generate a variety of memory elements (e.g., accelerator local memories, multi-port caches, and memory IPs) that can be easily integrated in different commercial synthesis flows for heterogeneous architecture design.

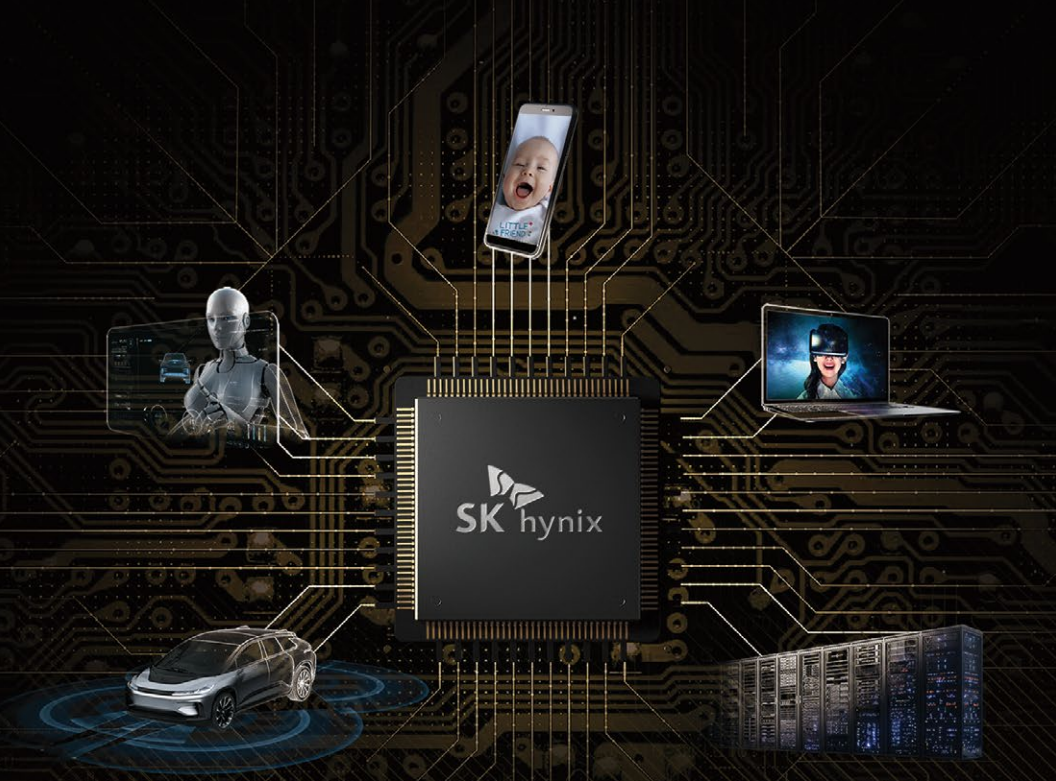
Biographies:

Christian Pilato is a Post-Doctoral Researcher at Università della Svizzera Italiana (USI), Switzerland. He holds a Ph.D. in Information Technology from Politecnico di Milano, Italy. From 2013 to 2016, he was a Post-Doctoral Research Scientist at Columbia Univ., USA. He has been also visiting researcher at NanGate, Chalmers Univ. of Technology, and Delft Univ. of Technology. His current research interests include high-level synthesis and heterogeneous architectures, with emphasis on memory and security aspects. Dr. Pilato was the Program Chair of EUC 2014. He has contributed to several projects sponsored by European Union, DARPA, and a research center supported by SRC.

Luca Carloni is an Associate Professor of Computer Science at Columbia Univ.. He received the Laurea degree (summa cum laude) in electrical engineering from the Università di Bologna and the M.S. and Ph.D. degrees in electrical engineering and computer sciences from the Univ. of California at Berkeley. His research interests include system-on-chip platforms and embedded systems. He has authored over 130 publications. He received the Faculty Early Career Development (CAREER) Award from the NSF in 2006, the Alfred P. Sloan Research fellowship in 2008, and the ONR Young Investigator Award in 2010. He is a Fellow of the IEEE.

Speakers:

Christian Pilato - *Univ. della Svizzera Italiana,*
Luca P. Carloni - *Columbia Univ.*



Thousands. Millions. Billions.
Trillions of times a second.
Matter that transforms what matters,
to make a difference in the world.

To most people,
they're just "semiconductors."
To SK Hynix,
they are "that very change."

That change starts within

Create the outside from within

SK hynix

MONDAY, OCTOBER 16 SCHEDULE OF EVENTS

	Crystal 1	Crystal 2	Crystal 3	Emerald
08:15 - 09:00	**ESWEEK Opening Session** | Room: Crystal			
09:00 - 10:00	**Monday Keynote:** *Kurt Keutzer, Univ. of California, Berkeley, Small Neural Nets Are Beautiful: Enabling Embedded Systems with Small Deep-Neural-Network Architectures* | Room: Crystal			
10:00 - 10:30	Coffee Break | Room: Crystal Foyer			
10:30 - 12:00	**CASES:** *Compilers Rising to Emerging Challenges*	**CODES+ISSS:** *Security*	**EMSOFT:** *Scheduling and Isolation*	**CODES+ISSS:** *Flash Memories I*
12:00 - 12:30	**Poster Session** | Room: Crystal Foyer			
12:30 - 13:30	Lunch | Room: Sapphire			
13:30 - 15:00	**CASES:** *Spotlight on Multi-cores: Dynamic Adaptation and Scheduling*	**Special Session CODES+ISSS:** *Challenges and Opportunities in Lattice Based Cryptography*	**EMSOFT:** *Verification*	**CODES+ISSS:** *Flash Memories II*
15:00 - 15:30	**Poster Session** | Room: Crystal Foyer			
15:30 - 17:00	**Special Session CASES:** *Approximate Computing: Trends, Challenges, and the Research Roadmap!*	**CODES+ISSS:** *Security, Reliability and Safety*	**EMSOFT:** *Cyber-Physical Systems*	**CODES+ISSS:** *GPU-based Systems*
17:00 - 17:30	**Poster Session** | Room: Crystal Foyer			
19:00	**Technical Program Committee Dinner** | Samcheonggak Restaurant			

Opening Session

Time: 08:15 - 09:00 | Room: Crystal

Keynote: Small Neural Nets Are Beautiful: Enabling Embedded Systems with Small Deep-Neural-Network Architectures

Time: 09:00 - 10:00 | Room: Crystal

Keynote Speaker:
Kurt Keutzer - *Univ. of California, Berkeley*

Over the last 50 years, in the diverse areas of natural language processing, speech recognition and computer vision, progress has been achieved through the orchestration of dozens of algorithms generally classified under the heading of "machine learning." In just the last five years the best results on most of the problems in these areas have been provided by a single general approach: Deep Neural Networks (DNNs). Moreover, for many problems, such as object classification and object detection, results using DNNs enabled computer vision algorithms to offer an acceptable level of accuracy for the first time. Thus, in many application areas, broader algorithmic exploration is being replaced by the creation of a single DNN architecture. Compared to other software architectures DNNs are quite simple. They consist of a simple feedforward pipe-and-filter structure. Nevertheless, the particular organization of the DNN and the precise characterization of the computations in the filter elements is diverse enough to create a rich design space. In the creation of a DNN to solve a particular application problem there are two implicit questions:

1) What is the right DNN architecture?

2) How do we find the right DNN architecture?

Our prior work in embedded systems has led us to explore these questions in a couple novel ways. First, for us "the right" DNN is one that offers acceptable accuracy and is capable of operating in real-time within the power and energy constraints of its target embedded application. This focus has led us away from experimenting with DNN architectures with a large number (e.g. 60M) of model parameters because their memory footprint makes them prohibitively expensive for deployment in many embedded systems. Instead we opted to explore the other extreme: very small DNN architectures capable of fitting into even the smallest embedded systems.

In approaching the second question, "What is the right DNN architecture?" we sought to leverage decades of research on systematic design-space exploration of application-specific embedded microprocessors.

The first result of our efforts was SqueezeNet, a DNN targeted for the object classification problem that achieves the same accuracy as the popular DNN AlexNet but with a 50x reduction in the number of model parameters. In this talk we will discuss our systematic approach to the creation of SqueezeNet and will broadly survey diverse efforts on designing small DNNs targeted for embedded systems.

Biography:
Kurt Keutzer is a Professor of Electrical Engineering and Computer Science at the Univ. of California, Berkeley. Prior to joining UC Berkeley he was Senior Vice-President and Chief Technical Officer at Synopsys. The 50th Design Automation Conference awarded Kurt a number of honors including "Top 10 Most Cited Author," and "Author of a Top 10 Most Cited Paper." He was also recognized as one of three people to have received four Best Paper Awards in the 50 Year History of the DAC. Kurt has been a Fellow of the IEEE since 1996. As an entrepreneur Kurt has been an active angel investor and was among the first investors in both Coverity and Tensilica. Kurt recently co-founded DeepScale with Forrest Iandola.

Kurt's current research interests are at the two ends of the computational spectrum of Deep Learning: accelerating the training of Deep Neural Nets using massively distributed computing, and designing and implementing Deep Neural Nets for embedded systems.

Session 1A - CASES: Compilers Rising to Emerging Challenges

Time: 10:30 - 12:00 | Room: Crystal 1

Chair:

Christophe Dubach - *Univ. of Edinburgh*

***1A.1 MODULAR COMPILATION OF HYBRID SYSTEMS FOR EMULATION AND LARGE SCALE SIMULATION**

Avinash Malik, Partha Roop - *Univ. of Auckland,*
Mark Trew - *Univ. of Auckland,*
Michael Mendler - *Univ. of Bamberg,*
Sidharta Andalam - *Univ. of Auckland*

1A.2 COMPLETE AND PRACTICAL UNIVERSAL INSTRUCTION SELECTION

Gabriel Hjort Blindell - *KTH Royal Institute of Technology,*
Mats Carlsson - *RISE SICS,*
Roberto Castañeda Lozano - *RISE SICS,*
Christian Schulte - *KTH Royal Institute of Technology*

1A.3 AN EFFICIENT WCET-AWARE INSTRUCTION SCHEDULING AND REGISTER ALLOCATION APPROACH FOR CLUSTERED VLIW PROCESSORS

Xuesong Su - *Univ. of New South Wales,*
Hui Wu - *Univ. of New South Wales,*
Jingling Xue - *Univ. of New South Wales*

Session 1B - CODES+ISSS: Security

Time: 10:30 - 12:00 | Room: Crystal 2

Chair:

Chengmo Yang - *Univ. of Delaware*

Co-Chair:

Hyunok Oh - *Handong Univ.*

***1B.1 CAMSURE: SECURE CONTENT-ADDRESSABLE MEMORY FOR APPROXIMATE SEARCH**

M. Sadegh Riazi, Mohammad Samragh, Farinaz Koushanfar - *Univ. of California, San Diego*

1B.2 EFFICIENT CONTROL-FLOW SUBGRAPH MATCHING FOR DETECTING HARDWARE TROJANS IN RTL MODELS

Luca Piccolboni - *Columbia Univ.,*
Alessandro Menon, Graziano Pravadelli - *Univ. of Verona*

1B.3 A HIGH-SPEED ACCELERATOR FOR HOMOMORPHIC ENCRYPTION USING THE KARATSUBA ALGORITHM

Vincent Migliore, Cédric Seguin, Maria Méndez Real, Vianney Lapotre, Arnaud Tisserand - *Univ. de Bretagne SUD,*
Caroline Fontaine - *IMT Atlantique,*
Russell Tessier - *Univ. of Massachusetts,*
Guy Gogniat - *Univ. de Bretagne SUD*

** Denotes Best Paper Candidate*

Session 1C - EMSOFT: Scheduling and Isolation

Time: 10:30 - 12:00 | Room: Crystal 3

Chair:

Wang Yi - *Uppsala Univ.*

1C.1 MC-ADAPT: ADAPTIVE TASK DROPPING WITH TASK-LEVEL MODE SWITCH IN MIXED-CRITICALITY SCHEDULING

Jaewoo Lee - *Univ. of Pennsylvania,*
Hoon Sung Chwa - *Univ. of Michigan,*
Linh Thi Xuan Phan - *Univ. of Pennsylvania,*
Insik Shin - *KAIST,*
Insup Lee - *Univ. of Pennsylvania*

1C.2 TIGHTENING CONTENTION DELAYS WHILE SCHEDULING PARALLEL APPLICATIONS ON MULTI-CORE ARCHITECTURES

Benjamin Rouxel, Isabelle Puaut, Steven Derrien - *Univ. of Rennes 1*

1C.3 ON THE DESIGN AND APPLICATION OF THERMAL ISOLATION SERVERS

Rehan Ahmed, Pengcheng Huang - *ETH Zurich,*
Lothar Thiele - *Swiss Federal Institute of Technology Zurich,*
Max Millen - *ETH Zurich*

Session 1D - CODES+ISSS: Flash Memories I

Time: 10:30 - 12:00 | Room: Emerald

Chair:

Dimitrios Soudris - *Univ. of Athens*

Co-Chair:

Soontae Kim - *KAIST*

1D.1 FLASHKV: ACCELERATING KV PERFORMANCE WITH OPEN-CHANNEL SSDS

Jiacheng Zhang, Youyou Lu, Jiwu Shu, Xiongjun Qin - *Tsinghua Univ.*

1D.2 P-BMS: A BAD BLOCK MANAGEMENT SCHEME IN PARALLELIZED FLASH MEMORY STORAGE DEVICES

Hong Seok Kim - *FADU Inc.,*
Sheayun Lee - *Kookmin Univ.,*
Sang Lyul Min - *Seoul National Univ.,*
Eyee Hyun Nam - *FADU Inc.,*
Ji Hyuck Yun - *SK Telecom*

1D.3 WORK IN PROGRESS: A UNIFIED FRAMEWORK FOR THROUGHPUT ANALYSIS OF SYNCHRONOUS DATA FLOW GRAPHS UNDER MEMORY CONSTRAINTS

Xue-Yang Zhu - *Chinese Academy of Sciences*

1D.4 WORK IN PROGRESS: IPAD: INTELLIGENT PV AWARE DATA PLACEMENT FOR READ PERFORMANCE IMPROVEMENT ON LDPC BASED FLASH MEMORY

Qiao Li, Liang Shi, Yejia Di - *Chongqing Univ.,*
Yajuan Du - *City Univ. of Hong Kong,*
Kaijie Wu - *Chongqing Univ.,*
Chun Jason Xue - *City Univ. of Hong Kong,*
Qingfeng Zhuge, Edwin H.-M. Sha - *Chongqing Univ.*

1D.5 WORK IN PROGRESS: EXPLORING FAST AND SLOW MEMORIES IN HMP CORE TYPES

Bryan Donyanavard - *Univ. of California, Irvine,*
Amir Mahdi Hosseini Monazzah - *Sharif Univ. of Technology,*
Tiago Muck, Nikil Dutt - *Univ. of California, Irvine*

1D.6 WORK IN PROGRESS: ALERT-AND-TRANSFER: AN EVOLUTIONARY ARCHITECTURE FOR SSD-BASED STORAGE SYSTEMS

Yue Zhu, Fei Wu, Qin Xiong, Changsheng Xie - *Huazhong Univ. of Science and Technology*

Poster Session

Time: 12:00 - 12:30 | Room: Crystal Foyer

* *Denotes Best Paper Candidate*

Session 2A - CASES: Spotlight on Multi-cores: Dynamic Adaptation and Scheduling

Time: 13:30 - 15:00 | Room: Crystal 1

Chair:

Sri Parameswaran - *Univ. of New South Wales*

2A.1 A STUDY OF DYNAMIC PHASE ADAPTATION USING A DYNAMIC MULTICORE PROCESSOR

Paul-Jules Micolet - *Univ. of Edinburgh,*
Aaron Smith - *Microsoft Research,*
Christophe Dubach - *Univ. of Edinburgh*

2A.2 IMPLEMENTATION OF PARTITIONED MIXED-CRITICALITY SCHEDULING ON A MULTI-CORE PLATFORM

Roman Trüb, Georgia Giannopoulou, Andreas Tretter, Lothar Thiele - *ETH Zurich*

2A.3 DYPO: DYNAMIC PARETO OPTIMAL CONFIGURATION SELECTION FOR HETEROGENEOUS MPSOCS

Ujjwal Gupta, Chetan Arvind Patil, Ganapati Bhat - *Arizona State Univ.,*
Prabhat Mishra - *Univ. of Florida,*
Umit Ogras - *Arizona State Univ.*

Session 2B - Special Session CODES+ISSS: Challenges and Opportunities in Lattice Based Cryptography

Time: 13:30 - 15:00 | Room: Crystal 2

Chair:

Francesco Regazzoni - *ALaRI*

Organizers:

Francesco Regazzoni - *ALaRI,*
Elizabeth O'Sullivan - *Queen's Univ. Belfast*

2B.1 TRENDS, CHALLENGES AND NEEDS FOR LATTICE-BASED CRYPTOGRAPHY IMPLEMENTATIONS

Hamid Nejatollahi, Nikil Dutt - *Univ. of California, Irvine,*
Rosario Cammarota - *Qualcomm Research*

2B.2 EFFICIENT ARITHMETIC FOR LATTICE-BASED CRYPTOGRAPHY

Elizabeth O'Sullivan - *Queen's Univ. Belfast,*
Francesco Regazzoni - *ALaRI*

2B.3 HAMPERING FAULT ATTACKS AGAINST LATTICE-BASED SIGNATURE SCHEMES - COUNTERMEASURES AND THEIR EFFICIENCY

Nina Bindel, Johannes Schreiber, Juliane Krämer - *Technische Univ. Darmstadt*

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Session 2C - EMSOFT: Verification

Time: 13:30 - 15:00 | Room: Crystal 3

Chair:
Robert de Simone - *Inria*

2C.1 A FAST METHOD TO COMPUTE DISJUNCTIVE QUADRATIC INVARIANTS OF NUMERICAL PROGRAMS
Xavier Allamigeon, Stephane Gaubert - *INRIA,*
Eric Goubault - *LIX, Ecole Polytechnique,*
Sylvie Putot - *LIX, Ecole polytechnique,*
Nikolas Stott - *INRIA*

2C.2 IMPROVING INVARIANT MINING VIA STATIC ANALYSIS
Christoph Schulze, Rance Cleaveland - *Univ. of Maryland*

2C.3 FORMAL VERIFICATION OF A TIMING ENFORCER IMPLEMENTATION
Sagar Chaki, Dionisio de Niz - *Carnegie Mellon Univ.*

Session 2D - CODES+ISSS: Flash Memories II

Time: 13:30 - 15:00 | Room: Emerald

Chair:
Rainer Dömer - *Univ. of California, Irvine*

Co-Chair:
Chengmo Yang - *Univ. of Delaware*

2D.1 A PROGRAM INTERFERENCE ERROR AWARE LDPC SCHEME FOR IMPROVING NAND FLASH DECODING PERFORMANCE
Fei Wu - *Wuhan National Laboratory for Optoelectronics,*
Meng Zhang, Yajuan Du - *Huazhong Univ. of Science and Technology,*
Xubin He - *Temple Univ.,*
Ping Huang - *Temple Univ.,*
Changsheng Xie, Jiguang Wan - *Wuhan National Laboratory for Optoelectronics*

2D.2 P-ALLOC: PROCESS-VARIATION TOLERANT RELIABILITY MANAGEMENT FOR 3D CHARGE-TRAPPING FLASH MEMORY
Yi Wang, Lisha Dong, Rui Mao - *Shenzhen Univ.,*

2D.3 WORK IN PROGRESS: DOVE: PINPOINTING FIRMWARE SECURITY VULNERABILITIES VIA SYMBOLIC CONTROL FLOW ASSERTION MINING
Alessandro Danese, Graziano Pravadelli - *Univ. of Verona,*
Valeria Bertacco - *Univ. of Michigan*

2D.4 WORK IN PROGRESS: REMOTE DETECTION OF UNAUTHORIZED ACTIVITY VIA SPECTRAL ANALYSIS
Fatih Karabacak, Umit Ogras, Sule Ozev - *Arizona State Univ.*

2D.5 WORK IN PROGRESS: COMMUNICATION OPTIMIZATION FOR THERMAL RELIABLE MANY-CORE SYSTEMS
Lei Yang, Weichen Liu, Weiwen Jiang - *Chongqing Univ.,*
Nan Guan - *Hong Kong Polytechnic Univ.*

2D.6 WORK IN PROGRESS: TOWARDS THE APPLICATION OF FLASK SECURITY ARCHITECTURE TO SOC DESIGN
Festus Hategekimana, Christophe Bobda - *Univ. of Arkansas*

Poster Session

Time: 15:00 - 15:30 | Room: Crystal Foyer

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Session 3A - Special Session CASES: Approximate Computing: Trends, Challenges, and the Research Roadmap!

Time: 15:30 - 17:00 | Room: Crystal 1

Chair:
Lukas Sekanina - *Brno Univ. of Technology*

Organizers:
Muhammad Shafique - *Technische Univ. Wien,*
Anand Ragunathan - *Purdue Univ.*

The goal of this special session is on exposing the challenges for Approximate Computing across various layers of the hardware-software stacks in order to enable cross-layer approximate computing, along with an overview of the early research efforts. This special session highlights the new challenges and opportunities available at multiple abstraction levels and motivates the need to bridge this gap.

3A.1 A QUANTIFIABLE APPROACH TO APPROXIMATE COMPUTING
Sachin Sapatnekar - *Univ. of Minnesota*

3A.2 QUALITY-CONFIGURABLE MEMORY HIERARCHY THROUGH APPROXIMATION
Nikil Dutt, Majid Shoushtari, Amir M. Rahmani - *Univ. of California, Irvine*

3A.3 HARDWARE APPROXIMATE COMPUTING: WHY, HOW, WHEN AND WHERE
Sri Parameswaran, Hassaan Saadat - *Univ. of New South Wales*

3A.4 PROBABILISTIC REASONING FOR ANALYSIS OF APPROXIMATE COMPUTATIONS
Sasa Misailovic - *Univ. of Illinois*

Session 3B - CODES+ISSS: Security, Reliability and Safety

Time: 15:30 - 17:00 | Room: Crystal 2

Chair:
Tosiron Adegbija - *Univ. of Arizona*

Co-Chair:
Francesco Regazzoni - *ALaRI*

3B.1 AN AUTOMATED SECURITY-AWARE APPROACH FOR DESIGN OF EMBEDDED SYSTEMS ON MPSOC
Benjamin Tan, Morteza Biglari-Abhari, Zoran Salcic - *Univ. of Auckland*

3B.2 SOFTRM: SELF-ORGANIZED FAULT-TOLERANT RESOURCE MANAGEMENT FOR FAILURE DETECTION AND RECOVERY IN NOC BASED MANY-CORES
Vasileios Tsoutsouras, Dimosthenis Masouros, Sotirios Xydis, Dimitrios Soudris - *National Technical Univ. of Athens*

3B.3 POWER-TEMPERATURE STABILITY AND SAFETY ANALYSIS FOR MULTIPROCESSOR SYSTEMS
Ganapati Bhat - *Arizona State Univ.,*
Suat Gumussoy - *IEEE Member,*
Umit Y. Ogras - *Arizona State Univ.*

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Session 3C - EMSOFT: Cyber-Physical Systems

Time: 15:30 - 17:00 | Room: Crystal 3

Chair:

Timothy Bourke - *INRIA*

3C.1 TIMESTAMP TEMPORAL LOGIC (TTL) FOR TESTING THE TIMING OF CYBER-PHYSICAL SYSTEMS

Mohammadreza Mehrabian, Mohammad Khayatian, Aviral Shrivastava - *Arizona State Univ.,*
John Eidson - *Univ. of California, Berkeley,*
Patricia Derler - *National Instruments,*
Hugo Andrade - *National Instruments Corp.,*
Li-Baboud Ya-Shian, Edward Griffor, Marc Weiss - *National Institute of Standards and Technology,*
Kevin Stanton - *Intel Corp.*

3C.2 TESTING CYBER-PHYSICAL SYSTEMS THROUGH BAYESIAN OPTIMIZATION

Jyotirmoy Deshmukh - *Toyota Technical Center,*
Marko Horvat - *MPI-SWS,*
Xiaoqing Jin - *Toyota Motor North America Research & Design,*
Rupak Majumdar, Vinayak Prabhu - *MPI-SWS*

3C.3 WORK IN PROGRESS: TESTING AUTONOMOUS CYBER-PHYSICAL SYSTEMS USING FUZZING FEATURES DERIVED FROM CONVOLUTIONAL NEURAL NETWORKS

Sunny Raj, Sumit Kumar Jha - *Univ. of Central Florida,*
Laura Pullum, Arvind Ramanathan - *Oak Ridge National Laboratory*

3C.4 WORK IN PROGRESS: VERIFYING STABILITY GUARANTEES OF CONTROL SOFTWARE IMPLEMENTATIONS IN THE PRESENCE OF SENSOR LEVEL FAULTS

Saurav Kumar Ghosh, Debasmita Lohar, Dibyendu Das, Dey Soumyajit - *Indian Institute of Technology Kharagpur*

3C.5 WORK IN PROGRESS: SMARTDTM: SMART THERMAL MANAGEMENT FOR SMARTPHONES

Wook Song - *Samsung Electronics,*
Jihong Kim - *Seoul National Univ.*

3C.6 WORK IN PROGRESS: MODELLING PROBABILISTIC TIMING ANALYSIS

Bojan Nokovic, Emil Sekerinski - *McMaster Univ.*

Session 3D - CODES+ISSS: GPU-based Systems

Time: 15:30 - 17:00 | Room: Emerald

Chair:

Soonhoi Ha - *Seoul National Univ.*

Co-Chair:

Ann Gordon-Ross - *Univ. of Florida*

3D.1 CGPREDICT: EMBEDDED GPU PERFORMANCE ESTIMATION FROM SINGLE-THREADED APPLICATIONS

Siqi Wang, Guanwen Zhong, Tulika Mitra - *National Univ. of Singapore*

3D.2 ENERGY EFFICIENT RUN-TIME MAPPING AND THREAD PARTITIONING OF CONCURRENT OPENCL APPLICATIONS ON CPU-GPU MPSOCS

Amit Kumar Singh - *Univ. of Southampton,*
Alok Prakash - *Nanyang Technological Univ.,*
Karunakar Reddy Basireddy, Geoff Merrett, Bashir M Al-Hashimi - *Univ. of Southampton*

3D.3 GPU PERFORMANCE ESTIMATION USING SOFTWARE RASTERIZATION AND MACHINE LEARNING

Kenneth O'Neal, Philip Brisk - *Univ. of California, Riverside,*
Zack Waters, Ahmed Abousamra, Emily Shriver - *Intel Corp.*

Poster Session

Time: 17:00 - 17:30 | Room: Crystal Foyer

Technical Program Committee Dinner

Time: 19:00 - 21:00 | Room: Samcheonggak Restaurant

** Denotes Best Paper Candidate*

TUESDAY, OCTOBER 17
SCHEDULE OF EVENTS

	Crystal 1	Crystal 2	Crystal 3	Emerald
07:30 - 09:00	Breakfast | Room: Sapphire			
09:00 - 10:00	Tuesday Keynote: Feng Zhao, Haier, IoT From the Lab to the Real World | Room: Crystal			
10:00 - 10:30	Coffee Break | Room: Crystal Foyer			
10:30 - 12:00	**CASES:** *Deep Dive into Embedded Architectures*	**CODES+ISSS:** *High-level Synthesis*	**EMSOFT:** *Schedulability Analysis*	**IoT TRACK:** *Machine Learning for IoT*
12:00 - 12:30	**Poster Session** | Room: Crystal Foyer			
12:30 - 13:30	Lunch | Room: Sapphire			
13:30 - 15:00	**CASES:** *Cool Chips: Microfluidics and Neural Network Accelerators*	**CODES+ISSS:** *Memory Systems*	**EMSOFT:** *Synchronous Reactive Systems*	**IoT TRACK:** *Providing Guarantees in IoT Systems*
15:00 - 15:30	Poster Session | Room: Crystal Foyer			
15:30 - 17:00	**CASES:** *Energy-Efficient Approximate Computing*	**Special Session CODES+ISSS:** *Data Analytics Enables Energy-Efficiency and Robustness: From Mobile to Manycores, Datacenters, and Networks*	**EMSOFT:** *Empirical Evaluation*	**IoT TRACK:** *Energy Harvesting for IoT*
17:00 - 17:30	**Poster Session** | Room: Crystal Foyer			
19:00 - 21:00	**Social Event - Hotel Signiel, Lotte World Tower** | Grand Ballroom			

Keynote: IoT From the Lab to the Real World

Time: 9:00 - 10:00 | Room: Crystal

Keynote Speaker:
Feng Zhao - *Haier*

The manufacturing industry is going through a digital transform, from a pure device maker to a hybrid device+service provider. IoT promises to be the enabler for this transformation, connecting at one end the consumers and the other end the manufacturers and their vast resources. I will draw examples from Haier's practices in smart home and connected factories. Building upon the IoT and other advanced computing technologies, Haier's U+ Platform has driven the rapid iteration and introduction of new consumer experiences and drastically improved the manufacturing efficiency.

Biography:
Dr. Feng Zhao is Chief Technology Officer and Vice President at Haier, a world leader in consumer appliances and smart devices. He is responsible for Haier's advanced R&D and smart home products and solutions. Under Dr. Zhao's leadership, Haier has developed the world's leading U+ Smart Home Platform, providing consumers with the best-in-class smart home devices, software and services. Together with Haier's Connected Factory effort, Haier is leading the industry in the digital transform from a hardware-centric manufacturer to an Internet enabled platform.

Dr. Zhao is a leading authority on Internet of Things (IoT), having pioneered and developed some of the foundational technologies in IoT. Dr. Zhao was an Assistant Managing Director at Microsoft Research Asia during 2009-2015, responsible for hardware, mobile and sensing, software analytics, systems, and networking research areas. He and his team developed mobile and cloud solutions that advanced the state-of-the-art in computing and significantly impacted Microsoft product groups: accurate indoor navigation system, efficient Internet search index serving platform, interactive visual analytics for big data, software defined radio and data center networking technologies. Prior to joining MSR-Asia, Dr. Zhao was a Principal Researcher at Microsoft Research Redmond (2004-2009), and founded the Networked Embedded Computing Area. During this time, he led the team to develop the MSR sensor mote, Tiny Web Service, SenseWeb and SensorMap, Data Center Genome, JouleMeter, and GAMPS data compression. Dr. Zhao received his PhD in Computer Science from MIT, and taught at Stanford Univ. and Ohio State Univ.. He was a Principal Scientist at Xerox PARC and founded PARC's research effort in sensor networks. He served as the founding Editor-In-Chief of ACM Transactions on Sensor Networks. Dr. Zhao is an IEEE Fellow, and received a Sloan Research Fellowship and NSF and ONR Young Investigator Awards. He has authored or co-authored over 100 technical papers and books and has over 40 US patents issued. His work has been featured in news media such as BBC World News, BusinessWeek, and Technology Review.

Session 4A - CASES: Deep Dive into Embedded Architectures

Time: 10:30 - 12:00 | Room: Crystal 1

Chair:

Akash Kumar - *Technische Univ. Dresden*

4A.1 CLUSTER COMMUNICATION USING REGISTERS

Vignyan Reddy Kothinti Naresh - *Qualcomm Research,*
Dibakar Gope, Mikko Lipasti - *Univ. of Wisconsin Madison,*

***4A.2 AN OUT-OF-ORDER LOAD-STORE QUEUE FOR SPATIAL COMPUTING**

Lana Josipovic - *École Polytechnique Fédérale de Lausanne,*
Philip Brisk - *Univ. of California, Riverside,*
Paolo Ienne - *École Polytechnique Fédérale de Lausanne*

4A.3 WORK IN PROGRESS: EFFICIENT PULSED-LATCH IMPLEMENTATION FOR MULTIPORT REGISTER FILES

Wael Elsharkasy, Hasan Erdem Yantır - *Univ. of California, Irvine,*
Amin Khajeh - *Broadcom Limited,*
Ahmed Eltawil, Fadi Kurdahi - *Univ. of California, Irvine*

4A.4 WORK IN PROGRESS: A "HIGH RESILIENCE" MODE TO MINIMIZE SOFT ERROR VULNERABILITIES IN ARM CORTEX-R CPU PIPELINES

Xabier Iturbe - *ARM Research,*
Balaji Venu, John Penton, Emre Ozer - *ARM*

4A.5 WORK IN PROGRESS: BALANCED CACHE BYPASSING FOR CRITICAL WARP REDUCTION

Sungin Hong, Hyunjun Kim, Hwansoo Han - *Sungkyunkwan Univ.*

4A.6 WORK IN PROGRESS: SSS: SELF-AWARE SYSTEM-ON-CHIP USING STATIC-DYNAMIC HYBRID METHOD

Gaoming Du, Shibi Ma, Zhenmin Li - *Hefei Univ. of Technology,*
Zhonghai Lu - *KTH Royal Institute of Technology,*
Duoli Zhang, Yiming Ouyang, Minglun Gao - *Hefei Univ. of Technology*

** Denotes Best Paper Candidate*

Session 4B - CODES+ISSS: High-level Synthesis

Time: 10:30 - 12:00 | Room: Crystal 2

Chair:
Luciano Lavagno - *Politecnico di Torino*

Co-Chair:
Francesco Regazzoni - *ALaRI*

4B.1 USING EFFICIENT PATH PROFILING TO OPTIMIZE MEMORY CONSUMPTION OF ON-CHIP DEBUGGING FOR HIGH-LEVEL SYNTHESIS
Marco Lattuada, Fabrizio Fezzardi - *Politecnico di Milano*

4B.2 COSMOS: COORDINATION OF HIGH-LEVEL SYNTHESIS AND MEMORY OPTIMIZATION FOR HARDWARE ACCELERATORS
Luca Piccolboni, Paolo Mantovani, Giuseppe Di Guglielmo, Luca Carloni - *Columbia Univ.*

4B.3 WORK IN PROGRESS: IR-LEVEL ANNOTATION STRATEGY DEALING WITH AGGRESSIVE LOOP OPTIMIZATIONS FOR PERFORMANCE ESTIMATION IN NATIVE SIMULATION
Omayma Matoussi, Frédéric Pétrot - *TIMA Lab, CNRS/Grenoble INP/UJF*

4B.4 WORK IN PROGRESS: A MACHINE LEARNING-BASED APPROACH FOR POWER AND THERMAL MANAGEMENT OF NEXT-GENERATION VIDEO CODING ON MPSOCS
Arman Iranfar, Marina Zapater, David Atienza, - *École Polytechnique Fédérale de Lausanne,*

4B.5 WORK IN PROGRESS: DRIVING BEHAVIOR MODELING AND ESTIMATION FOR BATTERY OPTIMIZATION IN ELECTRIC VEHICLES
Korosh Vatanparvar, Sina Faezi, Igor Burago, Marco Levorato, Mohammad Al Faruque - *Univ. of California, Irvine*

4B.6 WORK IN PROGRESS: A POWER-EFFICIENT AND HIGH PERFORMANCE FPGA ACCELERATOR FOR CONVOLUTIONAL NEURAL NETWORKS
Lei Gong, Chao Wang, Xi Li, Fan Sun, Chongchong Xu, Yuntao Lu, Yiwei Zhang, Xuehai Zhou - *Univ. of Science and Technology of China*

4B.7 WORK IN PROGRESS: HETEROGENEOUS REDUNDANCY TO ADDRESS PERFORMANCE AND COST IN MULTI-CORE SIMT
Mona Naghashi - *Sharif Univ. of Technology,* Seyyed Hasan Mozafari - *McGill Univ.,* Shaahin Hessabi - *Sharif Univ. of Technology*

** Denotes Best Paper Candidate*

Session 4C - EMSOFT: Schedulability Analysis

Time: 10:30 - 12:00 | Room: Crystal 3

Chair:
Sophie Quinton - *INRIA*

4C.1 WEAKLY HARD SCHEDULABILITY ANALYSIS FOR FIXED PRIORITY SCHEDULING OF PERIODIC REAL-TIME TASKS
Youcheng Sun - *Univ. of Oxford*
Marco Di Natale - *Scuola Superiore S. Anna*

4C.2 RESPONSE-TIME ANALYSIS FOR TASK CHAINS WITH COMPLEX PRECEDENCE AND BLOCKING RELATIONS
Johannes Schlatow, Rolf Ernst - *TU Braunschweig*

4C.3 AN ABSTRACTION-REFINEMENT THEORY FOR THE ANALYSIS AND DESIGN OF REAL-TIME SYSTEMS
Philip Kurtin, Marco Bekooij - *Univ. of Twente*

Session 4D - IoT TRACK: Machine Learning for IoT

Time: 10:30 - 12:00 | Room: Emerald

Chair:
Nachiket Kapre - *Univ. of Waterloo*

4D.1 MACHINE INTELLIGENCE ON RESOURCE-CONSTRAINED IOT DEVICES: THE CASE OF THREAD GRANULARITY OPTIMIZATION FOR CNN INFERENCE
Mohammad Motamedi, Daniel Fong, Soheil Ghiasi - *Univ. of California, Davis*

4D.2 HICH: HIERARCHICAL FOG-ASSISTED COMPUTING ARCHITECTURE FOR HEALTHCARE IOT
Iman Azimi, Arman Anzanpour - *Univ. of Turku,*
Amir M. Rahmani - *Univ. of California, Irvine,*
Tapio Pahikkala - *Univ. of Turku,*
Marco Levorato - *Univ. of California, Irvine,*
Pasi Liljeberg - *Univ. of Turku,*
Nikil Dutt - *Univ. of California, Irvine*

4D.3 WORK IN PROGRESS: A FAST ONLINE SEQUENTIAL LEARNING ACCELERATOR FOR IOT NETWORK INTRUSION DETECTION
Hantao Huang, Rai Suleman Khalid,
Hao Yu - *Nanyang Technological Univ.*

4D.4 WORK IN PROGRESS: SOPIOT : SERVICE-ORIENTED PLATFORM FOR INTERNET OF THINGS
Hyunjae Lee, EunJin Jeong, Donghyun Kang, Jinmyeong Kim, Soonhoi Ha - *Seoul National Univ.*

4D.5 WORK IN PROGRESS: SNAPSHOT-BASED OFFLOADING FOR MACHINE LEARNING WEB APP
Hyuk-Jin Jeong, Soo-Mook Moon - *Seoul National Univ.*

4D.6 WORK IN PROGRESS: CLOUD-BASED MACHINE LEARNING FOR IOT DEVICES WITH BETTER PRIVACY
Hyeon Jae Lee, Soo Mook Moon - *Seoul National Univ.*

Poster Session

Time: 12:00 - 12:30 | Room: Crystal Foyer

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Session 5A - CASES: Cool Chips - Microfluidics and Neural Network Accelerators

Time: 13:30 - 15:00 | Room: Crystal 1

Chair:

Nachiket Kapre - *Univ. of Waterloo*

5A.1 DIAGONAL COMPONENT EXPANSION FOR FLOW-LAYER PLACEMENT OF FLOW-BASED MICROFLUIDIC BIOCHIPS

Brian Crites, Karen Kong, Philip Brisk - *Univ. of California, Riverside*

5A.2 SYNTHESIS OF ERROR-RECOVERY PROTOCOLS FOR MICRO-ELECTRODE-DOT-ARRAY DIGITAL MICROFLUIDIC BIOCHIPS

Mahmoud Elfar, Zhanwei Zhong, Zipeng Li, Krishnendu Chakrabarty, Miroslav Pajic - *Duke Univ.*

5A.3 WORK IN PROGRESS: INCREMENTAL TRAINING OF CNNS FOR USER CUSTOMIZATION

Mansureh S. Moghaddam, Barend Harris, Duseok Kang, Inpyo Bae, Euiseok Kim, Hyemi Min - *Seoul National Univ.,*
Hansu Cho - *Samsung Electronics,*
Sukjin Kim - *Samsung Electronics,*
Bernhard Egger, Soonhoi Ha, Kiyoung Choi - *Seoul National Univ.*

5A.4 WORK IN PROGRESS: PREDICTION BASED CONVOLUTION NEURAL NETWORK ACCELERATION

Yuan Yao, Zhonghai Lu - *KTH Royal Institute of Technology*

5A.5 WORK IN PROGRESS: OPTIMIZING DCNN FPGA ACCELERATOR DESIGN FOR HANDWRITTEN HANGUL CHARACTER RECOGNITION

Changdae Lee, Hanwool Park, Yechan Yoo, Yoonjin Park, Kang Yi - *Handong Global Univ.*

5A.6 WORK IN PROGRESS: A HIGH-PERFORMANCE FPGA ACCELERATOR FOR SPARSE NEURAL NETWORKS

Yuntao Lu, Lei Gong, Chongchong Xu, Fan Sun, Yiwei Zhang, Chao Wang, Xuehai Zhou - *Univ. of Science and Technology of China*

** Denotes Best Paper Candidate*

Session 5B - CODES+ISSS: Memory Systems

Time: 13:30 - 15:00 | Room: Crystal 2

Chair:
Fabrizio Ferrandi - *Politecnico di Milano*

Co-Chair:
Umit Ogras - *Arizona State Univ.*

***5B.1 NUCLEUS: FINDING THE SHARING LIMIT OF HETEROGENEOUS CORES**
Ilias Vougioukas - *Univ. of Southampton,*
Andreas Sanberg, Stephan Diestelhorst - *ARM Ltd.,*
Bashir Al-Hashimi, Geoff Merrett - *Univ. of Southampton*

5B.2 EDGE-TM: EXPLOITING TRANSACTIONAL MEMORY FOR ERROR TOLERANCE AND ENERGY EFFICIENCY
Dimitra Papagiannopoulou - *Brown Univ.,*
Andrea Marongiu - *ETH Zurich,*
Tali Moreshet - *Boston Univ.,*
Maurice Herlihy, R. Iris Bahar - *Brown Univ.*

5B.3 EFFICIENT VIRTUAL MEMORY SHARING VIA ON-ACCELERATOR PAGE TABLE WALKING IN HETEROGENEOUS EMBEDDED SOCS
Pirmin Vogel, Andreas Kurth, Johannes Weinbuch - *ETH Zurich,*
Andrea Marongiu - *Swiss Federal Institute of Technology in Zurich,*
Luca Benini - *Università di Bologna*

Session 5C - EMSOFT: Synchronous Reactive Systems

Time: 13:30 - 15:00 | Room: Crystal 3

Chair:
Florence Maraninchi - *Verimag*

***5C.1 OPTIMIZATION OF REAL-TIME SOFTWARE IMPLEMENTING MULTI-RATE SYNCHRONOUS FINITE STATE MACHINES**
Yecheng Zhao - *Virginia Polytechnic Institute and State Univ.,*
Chao Peng - *National Univ. of Defense Technology,*
Haibo Zeng - *Virginia Polytechnic Institute and State Univ.,*
Zonghua Gu - *Zhejiang Univ.*

5C.2 A SYNCHRONOUS LOOK AT THE SIMULINK STANDARD LIBRARY
Timothy Bourke - *INRIA,*
Francois Carcenac, Jean-Louis Colaco, Bruno Pagano, Cédric Pasteur - *ANSYS/Esterel-Technologies,*
Marc Pouzet - *Ecole normale supérieure*

5C.3 TIMING ANALYSIS OF SYNCHRONOUS PROGRAMS USING WCRT ALGEBRA: SCALABILITY THROUGH ABSTRACTION
JiaJie Wang - *Univ. of Auckland,*
Michael Mendler - *Univ. of Bamberg,*
Partha Roop - *Univ. of Auckland,*
Bruno Bodin - *Univ. of Edinburgh*

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Session 5D - IoT TRACK: Providing Guarantees in IoT Systems

Time: 13:30 - 15:00 | Room: Emerald

Chair:
Aviral Shrivastava - *Arizona State Univ.*

***5D.1 LOW-COST MEMORY FAULT TOLERANCE FOR IoT DEVICES**
Mark Gottscho, Irina Alam, Clayton Schoeny, Lara Dolecek, Puneet Gupta - *Univ. of California, Los Angeles*

5D.2 RUNTIME ENFORCEMENT OF CYBER-PHYSICAL SYSTEMS
Srinivas Pinisetty - *Aalto Univ.,*
Partha Roop - *Univ. of Auckland,*
Steven Smyth - *Univ. of Kiel,*
Nathan Allen - *Univ. of Auckland,*
Stavros Tripakis - *Univ. of California, Berkeley,*
Reinhard von Hanxleden - *Univ. of Kiel*

5D.3 WORK IN PROGRESS: TOWARDS INDUSTRY STRENGTH MAPPING OF AUTOSAR\AUTOMOTIVE FUNCTIONALITY ON MULTICORE ARCHITECTURES
Cosmin Avasalcai, Dhanesh Budhrani, Paul Pop - *Technical Univ. of Denmark*

5D.4 WORK IN PROGRESS: RETENTION STATE-AWARE ENERGY MANAGEMENT FOR EFFICIENT NONVOLATILE PROCESSORS
Keni Qiu, Zhiyao Gong, Dongqin Zhou, Weiwen Chen - *Capital Normal Univ.,*
Yongpan Liu - *Tsinghua Univ.*

5D.5 WORK IN PROGRESS: JSDELTA: SERIALIZING MODIFIED JAVASCRIPT STATES FOR STATE SHARING
Jin-woo Kwon, Soo-Mook Moon - *Seoul National Univ.*

5D.6 WORK IN PROGRESS: INTEGRATING LOW-POWER IoT DEVICES TO A BLOCKCHAIN-BASED INFRASTRUCTURE
Kazım Rıfat Özyılmaz - *Boğaziçi Univ.,*
Arda Yurdakul - *Bogazici Univ.*

5D.7 WORK IN PROGRESS: CONTEXTUAL CALLBACKS FOR RESOURCE DISCOVERY AND TRUST NEGOTIATION ON THE INTERNET OF THINGS
Marten Lohstroh, Hokeun Kim - *Univ. of California, Berkeley,*
Edward A. Lee - *Univ. of California*

Poster Session

Time: 15:00 - 15:30 | Room: Crystal Foyer

Session 6A - CASES: Energy-Efficient Approximate Computing

Time: 15:30 - 17:00 | Room: Crystal 1

Chair:
Christian Pilato - *Univ. della Svizzera Italiana*

6A.1 APPROXIMATE MEMRISTIVE IN-MEMORY COMPUTING
Hasan Erdem Yantır, Ahmed M. Eltawil, Fadi Kurdahi - *Univ. of California, Irvine*

6A.2 ENERGY-EFFICIENT APPROXIMATE METAFUNCTIONS USING INPUT-AWARE QUANTIZED TABLE LOOKUP
Arnab Raha, Vijay Raghunathan - *Purdue Univ.*

6A.3 WORK IN PROGRESS: CODE-SIZE-AWARE MAPPING FOR SYNCHRONOUS DATAFLOW GRAPHS ON MULTICORE SYSTEMS
Mingze Ma, Rizos Sakellariou - *Univ. of Manchester*

6A.4 WORK IN PROGRESS: MULTI-GRAINED PERFORMANCE ESTIMATION FOR MPSOC COMPILERS
Miguel Angel Aguilar, Abishek Aggarwal, Awaid Shaheen, Rainer Leupers, Gerd Ascheid - *RWTH Aachen Univ.,*
Jeronimo Castrillon - *TU Dresden,*
Liam Fitzpatrick - *Silexica GmbH*

6A.5 WORK IN PROGRESS: REDEFINE - A CASE FOR WCET-FRIENDLY HARDWARE ACCELERATORS FOR REAL TIME APPLICATIONS
Kavitha Madhu, Tarun Singla, S K Nandy - *Indian Institute of Science,*
Ranjani Narayan - *Morphing Machines Pvt Ltd,*
Philippe Baufreton, Francois Neumann - *SAFRAN*

6A.6 WORK IN PROGRESS: ADVANCED AHEAD-OF-TIME COMPILATION FOR JAVASCRIPT ENGINE
HyukWoo Park, SungKook Kim, Soo-Mook Moon - *Seoul National Univ.*

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Session 6B - Special Session CODES+ISSS: Data Analytics Enables Energy-Efficiency and Robustness: From Mobile to Manycores, Datacenters, and Networks

Time: 15:30 - 17:00 | Room: Crystal 2

Chair:
Sudeep Pasricha - *Colorado State Univ.*

Organizer:
Sudeep Pasricha - *Colorado State Univ.,*

The amount of data generated and collected across computing platforms every day is not only enormous, but growing at an exponential rate. Advanced data analytics and machine-learning techniques have become increasingly essential to analyze and extract meaning from such "Big Data". These techniques can be very useful to detect patterns and trends to improve the operational behavior of computing platforms, but they also introduce a number of outstanding challenges: (1) How can we design and deploy data analytics and learning mechanisms to improve energy-efficiency in IoT and mobile devices, without introducing significant software overheads? (2) How to use machine learning and analytics techniques for effective design-space exploration during manycore chip design? (3) How can data analytics and learning improve the reliability and energy-efficiency of large-scale cloud datacenters, to cost-effectively support connected embedded and IoT platforms? (4) How can data analytics detect anomalies and increase robustness in the network backbone of emerging cloud datacenter networks? To address these outstanding challenges, out-of-the-box approaches need to be explored. In this special session, we will discuss the abovementioned outstanding problems and describe far-reaching solutions applicable across the interconnected ecosystem of IoT and mobile devices, manycore chips, datacenters, and networks. The special session brings together speakers with unique insights on applying data analytics and machine learning to real-world problems to achieve the most sought after features on multi-scale computing platforms, viz. intelligent data mining, energy-efficiency, and robustness. This special session will provide a holistic view on this emerging topic that encompasses machine learning, computing, and networking under a single umbrella.

6B.1 ENERGY-EFFICIENT AND ROBUST SOFTWARE DESIGN FOR EMERGING MOBILE AND CLOUD COMPUTING PLATFORMS: A DATA SCIENCE APPROACH
Sudeep Pasricha - *Colorado State Univ.*

6B.2 MACHINE LEARNING FOR DESIGN SPACE EXPLORATION AND OPTIMIZATION: TOWARDS COMPUTING AND PLANNING SUPPORT FOR MANYCORE SYSTEM-ON-CHIP DESIGN
Jana Doppa - *Washington State Univ.*

6B.3 TIME-SERIES DATA ANALYTICS FOR ANOMALY DETECTION IN TOMORROW'S NETWORK BACKBONE
Krishnendu Chakrabarty - *Duke Univ.*

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Session 6C - EMSOFT: Empirical Evaluation

Time: 15:30 - 17:00 | Room: Crystal 3

Chair:

Björn Brandenburg - *MPI for Software Systems, DE*

6C.1 BENCHPRIME: EFFECTIVE BUILDING OF A HYBRID BENCHMARK SUITE

Qingrui Liu, Xiaolong Wu, Larry Kittinger - *Virginia Tech,*
Markus Levy - *EEMBC,*
Changhee Jung - *Virginia Tech*

6C.2 DEMYSTIFYING SOFT-ERROR MITIGATION BY CONTROL-FLOW CHECKING - A NEW PERSPECTIVE ON ITS EFFECTIVENESS

Simon Schuster, Peter Ulbrich - *Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU),*
Isabella Stilkerich - *Schaeffler Technologies AG & Co. KG,*
Christian Dietrich - *Leibniz Univ. of Hannover,*
Wolfgang Schröder-Preikschat - *Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU)*

6C.3 WORK IN PROGRESS: COMBINING CONTROL FLOW CHECKING FOR SAFETY AND SECURITY IN EMBEDDED SOFTWARE

Robert Gold - *Technische Hochschule Ingolstadt*

6C.4 WORK IN PROGRESS: FIXED PRIORITY SCHEDULING OF REAL-TIME FLOWS WITH ARBITRARY DEADLINES ON DYNAMICALLY RECONFIGURABLE NOCS

Weichen Liu - *Nanyang Technological Univ.,*
Peng Chen, Lei Yang, Mengquan Li - *Chongqing Univ.,*
Nan Guan - *Hong Kong Polytechnic Univ.*

6C.5 WORK IN PROGRESS: CALMAR: A MULTI-APPLICATION DATAFLOW RUNTIME

Lionel Morel - *Université de Lyon,*
Manuel Selva, Tanguy Risset,
Kevin Marquet - *INRIA*

6C.6 WORK IN PROGRESS: EFFECTIVE SIMULATION OF DRAM/PCM-BASED HYBRID MEMORY

Xiaoliang Wang, Dezhi Zhang, Lihua Yue - *Univ. of Science and Technology of China*

Session 6D - IoT TRACK: Energy Harvesting for IoT

Time: 15:30 - 17:00 | Room: Emerald

Chair:

Naehyuck Change - *Korea Advanced Institute of Science and Technology*

6D.1 A DWM-BASED STACK ARCHITECTURE IMPLEMENTATION FOR ENERGY HARVESTING SYSTEMS

Hoda Aghaei Khouzani, Chengmo Yang - *Univ. of Delaware*

***6D.2 FLEXIBLE PV-CELL MODELING FOR ENERGY HARVESTING IN WEARABLE IOT APPLICATIONS**

Jaehyun Park, Hitesh Joshi - *Arizona State Univ.,*
Hyung Gyu Lee - *Daegu Univ.,*
Sayfe Kiaei, Umit Ogras - *Arizona State Univ.*

6D.3 ADAPTIVE POWER MANAGEMENT IN SOLAR ENERGY HARVESTING SENSOR NODE USING REINFORCEMENT LEARNING

Shaswot Shresthamali, Masaaki Kondo, Hiroshi Nakamura - *Univ. of Tokyo*

Poster Session

Time: 17:00 - 17:30 | Room: Crystal Foyer

Social Event - Hotel Signiel, Lotte World Tower

Time: 19:00 - 21:00 | Room: Grand Ballroom

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WEDNESDAY, OCTOBER 18
SCHEDULE OF EVENTS

	Crystal 1	Crystal 2	Crystal 3
07:30 - 08:30	Breakfast | Room Sapphire		
08:30 - 09:30	Wednesday Keynote: Gernot Heiser, Univ. of New South Wales: "Trustworthy Operating Systems for Critical Embedded and Cyberphysical Systems" | Room: Crystal		
09:30 - 10:00	Coffee Break | Room: Crystal Foyer		
10:30 - 11:30	**Special Session CASES:** *Emerging (Un-)Reliability Based Security Threats and Mitigations for Embedded Systems*	**CODES+ISSS:** *Cyber-Physical Systems*	**EMSOFT:** *Efficient Execution*
11:30 - 12:00	**Poster Session** | Room: Crystal Foyer		
12:00 - 13:00	Lunch | Room: Sapphire		
13:00 - 14:30	**CASES:** *The Future of Mobile Devices*	**Special Session CODES+ISSS:** *Approximate Computing for Scalable and Energy Efficient Embedded Systems*	**EMSOFT:** *Hybrid Systems*
14:30 - 15:00	Poster Session | Room: Crystal Foyer		
15:00 - 16:30	**CASES:** *Memory Boost Through Smart Management*	**CODES+ISSS:** *Scheduling*	**EMSOFT:** *Coordinating Robots and Control Tasks*
16:30 - 17:00	**Poster Session** | Room: Crystal Foyer		
17:00 - 17:30	Best Paper Awards Ceremony: | Room: Crystal		
17:30 - 18:30	**Panel Machine Learning for Embedded Systems: Hype or Lasting Impact?** Room: Crystal		

Keynote: Trustworthy Operating Systems for Critical Embedded and Cyberphysical Systems

Time: 08:30 - 09:30 | Room: Crystal

Keynote Speaker:
Gernot Heiser - *Univ. of New South Wales*

With the spread of cyberphysical systems and the IoT, trustworthiness of these devices, i.e. security, safety and dependability, is becoming increasingly important. Trustworthiness of non-trivial systems is critically dependent on the operating system (OS) enforcing isolation between components. However, traditional OS technology fails spectacularly to provide such isolation, resulting in the deluge of cyber-attacks we are experiencing. Such attacks are becoming a serious threat to economic stability and the functioning of society.

This talk will discuss the technical requirements for OSes for safety- and security-critical systems. It will present the seL4 microkernel as the system that goes furthest in supporting these requirements. Specifically, seL4 has formal, machine-checked proofs of implementation correctness from a high-level functional specification to machine code, and proofs that the kernel is able to enforce spatial isolation, including provable absence of covert storage channels. The kernel supports temporal integrity enforcement designed to support mixed-criticality real-time systems, an important feature for emerging cyber-physical systems with co-located functionalities (verification of these features is in progress). Integration with AADL-based model-driven development tools support seL4's use in real-world systems. The talk will also discuss on-going work on ensuring temporal confidentiality, i.e. prevention of covert timing channels.

Biography:
Gernot Heiser is Scientia Professor and John Lions Chair of Operating Systems at UNSW Sydney and Chief Research Scientist at Data61, CSIRO. He has a 20-year track record of building high-performance operating-system microkernels as a minimal basis for trustworthy systems. He is the founder and past leader of Data61's Trustworthy Systems group, which pioneered large-scale formal verification of systems code, specifically the design, implementation and verification of the seL4 microkernel. His former company Open Kernel Labs, acquired by General Dynamics in 2012, marketed the OKL4 microkernel, which shipped on billions of mobile wireless chips and more recently ships on the secure enclave processor of all iOS devices. Heiser is a Fellow of the ACM, the IEEE and the Australian Academy of Technology and Engineering (ATSE).

Session 7A - Special Session CASES: Emerging (Un-)Reliability Based Security Threats and Mitigations for Embedded Systems

Time: 10:00 - 11:30 | Room: Crystal 1

Chair:
Kiyoung Choi - *Seoul National Univ.*

Organizer:
Ramesh Karri - *New York Univ.*

This special session addresses various aspects of emerging (un-)reliability based security threats and mitigations for embedded systems. In particular, we consider threats and migations related to aging and side channels. Aging effects can be used as a hardware attack mechanism by using voltage scaling or specially constructed instruction sequences to cause guardband violations, thereby degrading the processor. Short-term aging effects can be utilized to cause transient degradations of a device. An attacker can also use various network-based and hardware-level attacks to modify behavior of an embedded system. Side channels provide an effective and secure methodology to remotely monitor code execution on an embedded processor. In particular, we consider the thermal side channel, which can be utilized to remotely observe level of processor activity. Machine learning based techniques are discussed for anomaly detection from thermal side channel measurements.

7A.1 AGING AND THERMAL RELIABILITY IN EMBEDDED SYSTEMS
Jörg Henkel - *Karlsruhe Institute of Technology*

7A.2 MALICIOUS AGING OF EMBEDDED SYSTEMS
Ramesh Karri - *New York Univ.*

7A.3 THERMAL RELIABILITY AS A SIDECHANNEL IN EMBEDDED SYSTEMS
Farshad Khorrami - *New York Univ.*

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Session 7B - CODES+ISSS: Cyber-Physical Systems

Time: 10:00 - 11:30 | Room: Crystal 2

Chair:

Petru Eles - *Linkoping Univ., Sweden*

Co-Chair:

Qi Zhu - *Univ. of California, Riverside*

7B.1 A NOVEL EMULATION MODEL OF THE CARDIAC CONDUCTION SYSTEM

Sidharta Andalam, Nathan Allen, Avinash Malik, Partha Roop, Mark Trew - *Univ. of Auckland*

7B.2 RISE: AN AUTOMATED FRAMEWORK FOR REAL-TIME INTELLIGENT VIDEO SURVEILLANCE ON FPGA

Bita Darvish Rouhani - *Univ. of California, San Diego,*
Azalia Mirhoseini - *Rice Univ.,*
Farinaz Koushanfar - *Univ. of California, San Diego*

7B.3 AN INEXACT ULTRA-LOW POWER BIO-SIGNAL PROCESSING ARCHITECTURE WITH LIGHTWEIGHT ERROR RECOVERY

Soumya Basu, Loris Duch, Rubén Braojos - *École Polytechnique Fédérale de Lausanne,*
Giovanni Ansaloni, Laura Pozzi - *Univ. of Lugano,*
David Atienza - *École Polytechnique Fédérale de Lausanne*

Session 7C - EMSOFT: Efficient Execution

Time: 10:00 - 11:30 | Room: Crystal 3

Chair:

Rolf Ernst, Technische Universität Braunschweig

7C.1 APPLICATION-AWARE SWAPPING FOR MOBILE SYSTEMS

Sang-Hoon Kim - *Virginia Tech,*
Jinkyu Jeong, Jin-Soo Kim - *Sungkyunkwan Univ.*

7C.2 LIGHTWEIGHT DATA COMPRESSION FOR MOBILE FLASH STORAGE

Cheng Ji - *City Univ. of Hong Kong,*
Li-Pin Chang - *National Chiao Tung Univ.,*
Liang Shi, Congming Gao - *Chongqing Univ.,*
Chao Wu - *City Univ. of Hong Kong,*
Yuangang Wang - *Huawei Technologies Co. Ltd.,*
jason xue - *City Univ. of Hong Kong*

7C.3 MANAGING THE PERFORMANCE / ERROR TRADEOFF OF FLOATING-POINT INTENSIVE APPLICATIONS

Ramy Medhat - *Univ. of Waterloo,*
Mike Lam - *James Madison Univ.,*
Barry Rountree - *Lawrence Livermore National Lab,*
Borzoo Bonakdarpour, Sebastian Fischmeister - *Univ. of Waterloo*

Poster Session

Time: 11:30 - 12:00 | Room: Crystal Foyer

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Session 8A - CASES: The Future of Mobile Devices

Time: 13:00 - 14:30 | Room: Crystal 1

Chair:

Joerg Henkel - *Karlsruhe Institute of Technology*

8A.1 USER-AWARE FRAME RATE MANAGEMENT IN ANDROID SMARTPHONES

Begum Birsen Egilmez, Matthew Schuchhardt, Gokhan Memik - *Northwestern Univ.,*
Raid Ayoub, Niranjan Soundararajan, Michael Kishinevsky - *Intel Corp.*

8A.2 FLOWPAP AND FLOWRER: IMPROVING ENERGY EFFICIENCY AND PERFORMANCE FOR STT-MRAM-BASED HANDHELD DEVICES UNDER READ DISTURBANCE

Hao Yan - *Univ. of Texas at San Antonio,*
Lei Jiang - *Indiana Univ.,*
Lide Duan, Wei-Ming Lin, Eugene John - *Univ. of Texas at San Antonio*

8A.3 WORK IN PROGRESS : TOWARDS EFFICIENT QUANTIZED NEURAL NETWORK INFERENCE ON MOBILE DEVICES

Yaman Umuroglu, Magnus Jahre - *Norwegian Univ. of Science and Technology*

8A.4 WORK IN PROGRESS : IMPROVING NVME SSD I/O DETERMINISM WITH PCIE VIRTUAL CHANNEL

Seonbong Kim, Joon-Sung Yang - *Sungkyunkwan Univ.*

8A.5 WORK IN PROGRESS : ENABLING NVM-BASED DEEP LEARNING ACCELERATION USING NON-UNIFORM DATA QUANTIZATION

Hao Yan, Ethan C. Ahn, Lide Duan - *Univ. of Texas at San Antonio*

8A.6 WORK IN PROGRESS : ENABLING RELIABLE MAIN MEMORY USING STT-MRAM VIA RESTORE-AWARE MEMORY MANAGEMENT

Armin Haj Aboutalebi, Lide Duan - *Univ. of Texas at San Antonio*

** Denotes Best Paper Candidate*

Session 8B - Special Session CODES+ISSS: Approximate Computing for Scalable and Energy Efficient Embedded Systems

Time: 13:00 - 14:30 | Room: Crystal 2

Chair:

Terrence Mak - *Univ. of Southampton,*

Organizers:

Patti Davide - *Univ. of Catania,*
Terrence Mak - *Univ. of Southampton,*
Palesi Maurizio - *Univ. of Catania*

Energy-Efficient Image Processing using Significance-driven Adaptive Approximate Computing

With increasing resolutions the volume of data generated by image processing applications is escalating dramatically. As such, when coupled with real-time performance requirements, reducing energy consumption is proving highly challenging. In this paper, we propose a novel approach for image processing applications using significance-driven approximate computing. Core to our approach is the fundamental tenet that image data should be processed intelligently based on their informational value, i.e. significance. For the first time, we define the concept of significance in the context of image processing. We show how the complexity of data processing tasks can be drastically reduced when computing decisions are synergistically adapted to significance learning principles. Using these principles more significant data are processed at higher precision with higher operating frequencies, while those with less significance are processed at reduced precision at lower operating frequenàè ìùcies, while maintaining a given quality requirement. Two concrete case studies are used to evaluate the effectiveness of our approach: an application-specific hardware-based adaptive approximate image filter and a software-based variable-kernel based parallel convolution filter running on an Odroid XU-4 platform. We demonstrate that our approach reduces energy by up to 40% for a real-time performance requirement of 15 fps, when compared with the existing approaches that are agnostic of significance and quality/slash energy trade-offs.

Embedded Abundant-data Computing Enabled by Amalgamation, Acceleration and Approximation

The world's appetite for abundant-data computing such as deep learning has increased dramatically. The computational demands of these applications far exceed the capabilities of today's systems, especially for energy-constrained embedded systems. These demands cannot be met by isolated improvements in transistor technologies, memories, or integrated circuit (IC) architectures alone. Trans-formative nanosystems, which leverage the unique properties of emerging nanotechnologies to create new IC architectures, are required to deliver unprecedented functionality, performance, and energy efficiency. Our new nanosystems approach overcomes these challenges through recent advances across the computing stack: (a) highly energy-efficient logic and memory nanotechnologies; (b) Ultra-dense (e.g., monolithic) three-dimensional integration with fine-grained connectivity which enables new architectures for computation immersed in memory, (c) programmable accelerators that improve domain-specific computing energy efficiency, and, (d) approximation techniques for energy efficiency and error resilience. Compared to conventional approaches, our approach promises to improve energy efficiency of computing systems by several orders of magnitude, thereby paving a path toward embedded abundant-data computing (e.g., deep learning -- both training and inference -- on mobile devices and IoT nodes).

Navigating Accuracy-Energy Trade-offs for Hardware Acceleration

Hardware acceleration has emerged as a method of choice to improve the efficiency of systems that need to perform lots of data processing under stringent energy constraints, particularly for IoT and embedded systems. A critical component to maximizing the efficiency of hardware accelerators is to ensure that energy is not being wasted in producing overly accurate results. For instance, in most sensory or signal processing applications, using double precision floating point would certainly be overkill. This paper presents QAPPA, a Quality Autotuner for Precision Programmable Accelerators. QAPPA analyzes applications written in C++ and derives the precision requirements of each compute and arithmetic operations in the program. It utilizes a library of hardware models to predict energy and memory bandwidth savings at different application quality levels. We demonstrate the utility of QAPPA over 14 PERFECT kernels and show that QAPPA can derive minimal quantization settings from user-defined quality constraints to significantly improve the energy efficiency of fixed-function hardware accelerators.

* *Denotes Best Paper Candidate*

An Efficient Hardware Design for Cerebellar Models using Approximate Circuits

The superior controllability of the cerebellum of primates has motivated extensive interest in the development of computational cerebellar models. Many models have been applied to the motor control and image stabilization in robots. Usually, cerebellar models are computationally complex, so they have rarely been implemented in dedicated hardware. Instead, a cerebellar model is often implemented in a system using a central processing unit (CPU) or a graphic processing unit (GPU) with a high energy consumption and a long latency. To overcome these drawbacks, we propose a cerebellar model implemented in approximate computing circuits with a low hardware overhead and a high speed, leveraging the inherent error tolerance in the cerebellum. As basic arithmetic elements in a cerebellar model, approximate adders and multipliers are carefully evaluated for implementations in an adaptive filter to achieve a best trade-off of accuracy and hardware overhead. A saccade system, whose vestibulo-ocular reflex (VOR) is controlled by the cerebellum, is simulated to show the applicability and effectiveness of the cerebellar model implemented in approximate circuits.

8B.1 SIGNIFICANCE-DRIVEN ADAPTIVE APPROXIMATE COMPUTING FOR ENERGY-EFFICIENT IMAGE PROCESSING APPLICATIONS

Dave Burke, Dainius Jenkus, Issa Qiqieh, Rishad Shafik - *Newcastle Univ.,*
Shidhartha Das - *ARM Ltd.,*
Alex Yakovlev - *Newcastle Univ.*

8B.2 3D NANOSYSTEMS ENABLE EMBEDDED ABUNDANT-DATA COMPUTING

William Hwang, Mohamed M. Sabry Aly, Yash H. Malviya, Mingyu Gao, Tony F. Wu, Christos Kozyrakis, H.S. Philip Wong, Subhasish Mitra - *Stanford Univ.*

8B.3 EXPLOITING QUALITY-ENERGY TRADEOFFS WITH ARBITRARY QUANTIZATION

Thierry Moreau - *Univ. of Washington,*
Augusto Felipe - *Univ. of Campinas,*
Howe Patrick, Armin Alaghi, Luis Ceze - *Univ. of Washington*

8B.4 AN EFFICIENT HARDWARE DESIGN FOR CEREBELLAR MODELS USING APPROXIMATE CIRCUITS

Jie Han - *Univ. of Alberta*

Session 8C - EMSOFT: Hybrid Systems

Time: 13:00 - 14:30 | Room: Crystal 3

Chair:

Miroslav Pajic - *Duke Univ.*

8C.1 OPERATIONAL MODELS OF PIECEWISE-SMOOTH SYSTEMS

Andrew Sogokon - *Vanderbilt Univ.,*
Khalil Ghorbal - *INRIA,*
Taylor T Johnson - *Vanderbilt Univ.*

8C.2 PROBABILISTIC SAFETY VERIFICATION OF STOCHASTIC HYBRID SYSTEMS USING BARRIER CERTIFICATES

Chao Huang, Xin Chen - *Nanjing Univ.,*
Wang Lin - *Wenzhou Univ.,*
Zhengfeng Yang - *East China Normal Univ.,*
Xuandong Li - *Nanjing Univ.*

***8C.3 COMPOSITIONAL RELATIONAL ABSTRACTIONS FOR NONLINEAR HYBRID SYSTEMS**

Xin Chen, Sergio Mover, Sriram Sankaranarayanan - *Univ. of Colorado*

** Denotes Best Paper Candidate*

Poster Session

Time: 14:30 - 15:00 | Room: Crystal Foyer

Session 9A - CASES: Memory Boost Through Smart Management

Time: 15:00 - 16:30 | Room: Crystal 1

Chair:

Aviral Shrivastasa - *Arizona State Univ.*

9A.1 USING CRITICALITY OF GPU ACCESSES IN MEMORY MANAGEMENT FOR CPU-GPU HETEROGENEOUS MULTI-CORE PROCESSORS

Siddharth Rai, Mainak Chaudhuri - *Indian Institute of Technology Kanpur*

9A.2 REINFORCEMENT LEARNING-ASSISTED GARBAGE COLLECTION TO MITIGATE LONG TAIL LATENCY PROBLEM

Wonkyung Kang - *Seoul National Univ.,*
Dongkun Shin - *Sungkyunkwan Univ.,*
Sungjoo Yoo - *Seoul National Univ.*

9A.3 MINIMISING ACCESS CONFLICTS ON SHARED MULTI-BANK MEMORY

Andreas Tretter, Georgia Giannopoulou, Matthias Baer, Lothar Thiele - *ETH Zurich*

Session 9B - CODES+ISSS: Scheduling

Time: 15:00 - 16:30 | Room: Crystal 2

Chair:

Todor Stefanov - *Leiden Univ.*

Co-Chair:

Weichen Liu - *Chongqing Univ.*

9B.1 ONLINE SCHEDULING OF 2-RE-ENTRANT FLEXIBLE MANUFACTURING SYSTEMS

Joost van Pinxten, Umar Waqas, Marc Geilen, Twan Basten - *Eindhoven Univ. of Technology,*
Lou Somers - *Océ Technologies,*

9B.2 RESPONSE TIME ANALYSIS FOR SPORADIC SERVER BASED BUDGET SCHEDULING IN REAL TIME VIRTUALIZATION ENVIRONMENTS

Matthias Beckert, Rolf Ernst - *Technische Univ. Braunschweig*

9B.3 ROUND-TRIP DRAM ACCESS FAIRNESS IN 3D NOC-BASED MANY-CORE SYSTEMS

Xiaowen Chen - *National Univ. of Defense Technology,*
Zhonghai Lu - *KTH Royal Institute of Technology,*
Shuming Chen, Sheng Liu - *National Univ. of Defense Technology*

** Denotes Best Paper Candidate*

Session 9C - EMSOFT: Coordinating Robots and Control Tasks

Time: 15:00 - 16:30 | Room: Crystal 3

Chair:

Sriram Sankaranarayanan - *Univ. of Colorado*

***9C.1 SECURITY-AWARE SCHEDULING OF EMBEDDED CONTROL TASKS**

Vuk Lesi, Ilija Jovanov, Miroslav Pajic - *Duke Univ.*

9C.2 A STRUCTURED METHODOLOGY FOR PATTERN BASED ADAPTIVE SCHEDULING IN EMBEDDED CONTROL

Sumana Ghosh, Souradeep Dutta, Soumyajit Dey, Pallab Dasgupta - *Indian Institute of Technology Kharagpur*

9C.3 ANTLAB: A MULTI-ROBOT TASK SERVER

Ivan Gavran, Rupak Majumdar - *MPI-SWS,* Indranil Saha - *IIT Kanpur*

Poster Session

Time: 16:30 - 17:00 | Room: Crystal Foyer

Awards Ceremony

Time: 17:00 - 17:30 | Room: Crystal

Panel: Machine Learning for Embedded Systems: Hype or Lasting Impact?

Time: 17:30 - 18:30 | Room: Crystal

Moderator:

Rolf Ernst - *Technische Univ. Braunschweig*

Organizer:

X. Sharon Hu - *Univ. of Notre Dame*

Machine learning (ML), especially deep learning and neural networks, is attracting a lot of attention in a number of application domains including embedded systems. ML can offer alternative ways to exploit data and usage patterns for embedded system design. However, one may argue that the general ML ideas have been used in embedded system design for a long time. Furthermore, besides challenged by limited resources such as time, energy and memory, many embedded systems are also required to provide guaranteed services such as timing, security, and reliability. These requirements are intrinsically in conflict with the use of ML. It then begs the question whether ML can really lead to fundamental advances for embedded systems or will remain limited to a few clearly defined application scopes. In this panel, leading embedded system experts will "declare" and support their respective positions and challenge others' opposing positions. Audience is invited to join this active debate, which should lead to insights on the true potentials and limitations of exploiting ML for embedded systems.

Panelists:

Petru Eles - *Linköping Univ.,*
Gernot Heiser - *Univ. of New South Wales,*
Kurt Keutzer - *Univ. of California, Berkeley,*
Peter Seungyoon Song - *LG Electronics,*
Cong Zhao - *DJI*

** Denotes Best Paper Candidate*

WORKSHOP SCHEDULE

THURSDAY

CyPhy'17: Sixth Workshop on Design, Modeling and Evaluation of Cyber Physical Systems
Thursday, October 19 | Time: 08:30 - 17:00 | Room: Garnet, 37F

DECPS'17: 1st ESWeek Workshop on Declarative Embedded and Cyber-Physical Systems
Thursday, October 19 | Time: 08:30 - 17:00 | Room: Astor, 36F

WESE'17: Embedded and Cyber-Physical Systems Education
Thursday, October 19 | Time: 08:30 - 17:00 | Room: Garnet, 37F

CAFFE2 TUTORIAL: Real-time AI in the palm of your hand with Caffe2
Thursday, October 19 | Time: 17:00 - 18:00 | Room: Emerald 2F

FRIDAY

HENND'17: International Workshop on Highly Efficient Neural Networks Design
Friday, October 20 | Time: 08:30 - 17:00 | Room: Sapphire 1+2+3, 3F

SYMPOSIA SCHEDULE

THURSDAY

ESTIMedia Symposium: 15th IEEE Symposium on Embedded Systems for Real-time Multimedia
Thursday, October 19 | Room: Peacock, 36F

THURSDAY & FRIDAY

NOCS 2017: 11th International Symposium on Networks-on-Chip
Thursday, October 19 - Friday, October 20 | Room: Belle-vue, 36F

RSP Symposium: IEEE International Symposium on Rapid System Prototyping
Thursday, October 19 - Friday, October 20 | Room: Berkely, 36F

Workshop - Sixth Workshop on Design, Modeling and Evaluation of Cyber Physical Systems (CyPhy'17)

Time: 08:30 - 17:00 | Room: Garnet, 37F

Cyber physical systems (CPS) combine computing and networking power with physical components. They enable innovation in a wide range of domains including robotics; smart homes, vehicles, and buildings; medical implants; and future-generation sensor networks. CyPhy'17 brings together researchers and practitioners working on modeling, simulation, and evaluation of CPS, based on a broad interpretation of these areas, to collect and exchange expertise from a diverse set of disciplines. The workshop places particular focus on techniques and components to enable and support virtual prototyping and testing. Topics presented at the workshop include: mathematical foundations of CPS, specification and construction techniques for CPS, as well as case studies and tools for CPS.

Organizers:

William Harrison, *Univ. of Missouri*
Pavithra Prabhakar, *Kansas State Univ.*

Session 1. 09:00 - 10:00

Ichiro Hasuo. Keynote Address. Nonstandard Static Analysis: *Literal Transfer of Deductive Verification Frameworks from Discrete to Hybrid*.

Session 2. 10:30 – 12:00

Takashi Tomita, Daisuke Ishii, Toru Murakami, Shigeki Takeuchi and Toshiaki Aoki. *Template-Based Monte-Carlo Test Generation for Simulink Models.*

Shakiba Yaghoubi and Georgios Fainekos. *Local Descent for Temporal Logic Falsification of Cyber-Physical Systems.*

Daisuke Ishii, Alexandre Goldsztejn and Naoki Yonezaki. *Reliable Simulation and Monitoring of Hybrid Systems Based on Interval Analysis.*

Session 3. 13:30 - 15:00

Hokeun Kim, Edward A. Lee and Armin Wasicek. *An Integrated Simulation Tool for Computer Architecture and Cyber-Physical Systems.*

Jeongyoon Eo, Kang-Wook Kim and Chang-Gun Lee. *Memory Access Pattern-Aware DRAM Controller Design for Mixed-Criticality Systems.*

Chao Wang, Yuming Cheng, Lei Gong, Bo Wan, Aili Wang, Xi Li and Xuehai Zhou. *FPGA based Big Data Accelerator Design in Teaching Computer Architecture and Organization.*

15:30 - 16:30 Panel and Conclusion.

Workshop - The First ESWeek Workshop on Declarative Embedded and Cyber-Physical Systems (DECPS)

Time: 08:30 - 17:00 | Room: Astor, 36F

Declarative programming (functional, logic, rule-based, constraints, dataflow, and visual) has several advantages over imperative programming. For example, using the functional reactive programming (FRP) paradigm over the imperative programming style found in languages such as C/C++/C# and Java for implementing embedded and CPS software allows the programmer to intuitively describe safety-critical behaviors of the system, thus lowering the chance of introducing bugs in the design phase. Its stateless nature of execution does not require the use of synchronization primitives like mutexes and semaphores, thus reducing the complexity in programming. However, accurate response time analysis of FRP-based controllers remains a largely unexplored problem. Furthermore, efficient runtime architectures and execution platforms for FRP and programs implemented in other declarative languages are nearly absent. Virtualization and hierarchical scheduling need to be explored as well.

Program Chair

Albert M. K. Cheng, *Univ. of Houston*

Application Validation on RTDroid
Yin Yan, *State Univ. of New York at Buffalo*
Lukasz Ziarek, State Univ.y of New York at Buffalo

P-FRP Task Scheduling with Preemption Threshold
Jian Lin, *Univ. of Houston*
Albert M. K. Cheng, *Univ. of Houston*

Bounding Execution Resources for the Task Scheduling Problem in Cyber-Physical Systems
Vlad Radulescu, *Cuza Univ. of Iasi Stefan*
Andrei, *Lamar Univ.*
Albert M. K. Cheng, *Univ. of Houston*

Workshop - Embedded and Cyber-Physical Systems Education (WESE) 2017

Time: 08:30 - 17:00 | Room: Garnet, 37F

WESE – Workshop on Embedded and Cyber-Physical Systems Education The WESE workshop aims to bring researchers, educators, and industrial representatives together to assess needs and share design, research, and experiences in embedded and cyber-physical systems education. WESE addresses questions such as “What skills and capabilities are required by the engineers of tomorrow”, “How should the corresponding educational programs be formed”, and “How can effective pedagogic methods be introduced in this domain”?

WESE 2017 is the 13th workshop in this series and is organized in collaboration with EMSIG (www.emsig.net), ACM SIGBED (http://sigbed.blogspot.se/), CPSE-Labs (http://www.cpse-labs.eu/) and the ARTEMIS-IA (https://www.artemis-ia.eu). The first workshop was held in 2005 in Jersey City. In 2012, the term ”Cyber-Physical“ was added to the workshop name, but the acronym was not modified. The inclusion of Cyber-Physical systems in the scope has broadened the scope and promises to attract a broader community both in terms of paper contributors and attendants. Since 2009, proceedings are included in the ACM digital library.

Tutorial - Caffe2 Tutorial: Real-time AI in the palm of your hand with Caffe2

Time: 17:00 - 18:00 | Room: Emerald 2F

Organizer:

Jaeyoun Kim - *Facebook*

Speakers:

Bram Wasti - *Facebook*

Caffe2 is a lightweight and cross platform deep learning framework evolved from the previous Caffe. Facebook is bringing AI to the edge using Caffe2 to enable real-time AI and AR experiences for Facebook applications. At this Caffe2 tutorial, you will learn how Caffe2 can help you to deploy and run deep learning models in real-time on mobile (iOS/Android) and embedded devices (e.g. NVIDIA Jetson TX2).

Workshop - International Workshop on Highly Efficient Neural Networks Design (HENND)

Time: 08:30 - 17:00 | Room: Sapphire 1+2+3

Organizers:

Yiran Chen, *Duke Univ.*
Sungjoo Yoo, *Seoul National Univ.*

The International Workshop on Highly Efficient Neural Networks Design is a forum for presentations of state-of-the-art research in highly efficient neural networks design. The workshop will combine both keynote/invited oral presentations and posters of the papers accepted from regular submissions.

Keynote and oral presentations

* Keynote by Prof. Yoshua Bengio (Univ. of Montreal), titled "Towards End-to-End Trainable Hardware"

* Invited talks by experts from Baidu, Toshiba, Samsung Electronics, DeepHi, ETH, KAIST, etc.

We invite submissions of poster papers related to (but not limited to) the following topics:

* Algorithm optimization (e.g., tiny Yolo for object detection)

* Model compression (e.g., pruning and low rank approximation)

* Deep learning framework (e.g., Caffe2 or TensorFlow framework for mobile and embedded systems)

* On-device training (e.g., federated learning in Google)

* CPU/DSP/GPU architecture enhancements for neural networks (e.g., Tensor Core in V100)

* FPGA/ASIC accelerators for neural networks (e.g., zero-aware low precision CNN/RNN accelerator)

Accepted papers are invited to the submission to a special issue of SCI journal, Design Automation for Embedded Systems (DAEM), Springer.

Sponsored by:

Baidu 百度

HENND 2017 Workshop Advance Program

FRIDAY OCT 20, 2017

8:30-9:20 Keynote 1
Prof. Yoshua Bengio, Univ. of Montreal, Towards End-to-End Trainable Hardware

9:20-10:10 Keynote 2
Prof Hoi-Jun Yoo, KAIST, Mobile/Embedded Deep Neural Networks and Applications

10:10-10:30 Poster and Coffee
Submitted poster papers are presented as posters

10:30-12:30 Session 1
Dr. Kangwon Lee, SK Telecom, Developing an AI Computing Infra at SKT, a Leading Service Provider

Dr. Takashi Miyamori, Toshiba, Efficient Implementation of Deep Neural Network Hardware

Dr. Jian Ouyang, Baidu, Power-Efficient Deep Learning accelerator for Baidu Apollo

Dr. Jaeyoun Kim, Facebook, Caffe2: A New Lightweight, Modular, and Scalable Deep Learning Framework for mobile deep learning

12:30-13:30 Lunch and Poster

13:30-15:00 Session 2
Dr. Yongdeok Kim, Samsung Electronics, CNN optimizations on smartphones

Prof. Yu Wang, DeepHi, Efficient Deep Learning Processing Unit Design for FPGA/Edge

Prof. Onur Mutlu, ETH Zurich, FPGA-accelerated Dense Linear Machine Learning: A Precision-Convergence Trade-off

15:00-15:30 Poster and Coffee

15:30-17:00 Session 3
Prof. Junmo Kim, KAIST, A Gift from Knowledge Distillation: Fast Optimization, Network Minimization and Transfer Learning

Prof. Sungju Hwang, UNIST, SplitNet: Learning to Semantically Split Deep Networks for Parameter Reduction and Model Parallelization

Prof. Minsoo Ryu, POSTECH, Accelerator-Centric Systems for Scalable and Energy-Efficient Deep Learning

ESTIMEDIA SYMPOSIUM

Symposia - 15th IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia 2017)

Time: 08:30 - 17:00 | Room: Peacock, 36F

Multimedia and camera-based technologies play an important role in our daily life, and have become among the most relevant technological innovations. These technologies have proliferated into a wide range of application domains like Internet-of-Things (IoT), Cyber-Physical Systems (CPS), Healthcare and Medical Image Processing, Security, Consumer, etc. The evermore increasing computational and communication requirements demanded by current and next generation multimedia and image/video processing devices together with energy constraints which characterize portable devices require innovative design methodologies and tools. The IEEE/ACM ESTIMedia aims to bring together people from different multimedia and imaging-related research communities who have worked separately but did not interact sufficiently to address the challenges facing the design of hardware and software layers of such highly specialized multimedia and image/video processing systems.

ESTIMedia focuses on all challenges related to the design of hardware and software in highly specialized multimedia and image/video processing systems. Topics of interest include all aspects of the design and implementation process of embedded single and multi-processor systems. This includes (but is not limited to):

- Emerging trends for embedded multimedia systems (approximate computing, neuromorphic computing, embedded/mobile gaming, etc.)
- Application of camera-based processing in IoT, CPS, and Healthcare
- Real-time medical imaging
- Security and protection of media processing and streams
- Circuits and architectures for embedded multimedia and image/video processing systems
- Multimedia processors, reconfigurable architectures, many-core systems, and networks-on-chip
- Specification, modeling, design methodologies, and case studies
- Validation and verification of embedded multimedia and image/video processing systems
- Software optimization and compiler techniques
- Timing aspects of media streams
- Scheduling and analysis of media processing
- Resource and QoS management methods
- Real-time kernels, OS and middleware support

The full technical program can be found at www.estimedia.org/program

General Chair
Muhammad Shafique, *TU Wien*

Program Co-Chairs
Sander Stuijk, *Eindhoven Univ. of Technology*

Akash Kumar, *TU Dresden*

NOCS SYMPOSIUM

Symposia - 11th International Symposium on Networks-on-Chip (NOCS 2017)

Time: 08:30 - 17:30 | Room: Belle-vue, 36F

Chairs:

Zhonghai Lu - *KTH Royal Institute of Technology,*
Umit Ogras - *Arizona State Univ.*

Organizers:

Axel Jantsch - *Vienna Univ. of Technology,*
Hiroki Matsutani - *Keio Univ.*

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, chip-scale, and multichip package-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on NoC innovations and applications from inter-related research communities, including computer architecture, networking, circuits and systems, packaging, embedded systems, co-design, and design automation.

SCHEDULE:

Thursday - 8:30am to 5:30pm

Friday - 8:30am to 5:00pm

Sponsored by:

NOCS 2017 Program

THURSDAY OCT 19, 2017

[07.30 - 08.30] Breakfast

[08:30-08:45] Opening

Session chair: Umit Ogras (Arizona State University) and Zhonghai Lu (KTH Royal Institute of Technology)

[08:45-10:00] Keynote

Title: Networks Off Chip: High Performance Fabrics in Support of the Data Center Computer

Speaker: Robert Zak (Intel Corporation)

[10:00 – 10:30] Coffee Break

[10:30 – 12:30] Session 1: Efficient Router and NoC Architecture

Session chair: Hiroki Matsutani (Keio Univ.)

17 Minimally Buffered Deflection Routing with In-Order Delivery in a Torus

Authors: Jörg Mische, Christian Mellwig, Alexander Stegmeier, Martin Frieb and Theo Ungerer (Univ. of Augsburg)

34 Distributed and Dynamic Shared-Buffer Router for High-Performance Interconnect

Authors: Charles Effiong, Gilles Sassatelli and Abdoulaye Gamatie (LIRMM)

4 A Novel Approach to Reduce Packet Latency Increase caused by Power Gating in Network-on-Chip

Authors: Peng Wang, Sobhan Niknam (Leiden Univ.), Zhiying Wang (National Univ. of Defense Technology) and Todor Stefanov (Leiden Univ.)

29 Improving the Reliability and Energy-Efficiency of High-Bandwidth Photonic NoC Architectures with Multilevel Signaling

Authors: Ishan Thakkar, Sai Vineel Reddy Chittamuru and Sudeep Pasricha (Colorado State Univ.)

[12:30 – 13:30] Lunch Break

[13:30 – 15:00] Session 2: Interconnect Architecture and Heterogeneous System (Best paper candidates session)

Session chair: Axel Jantsch (TU Wien)

*43 Energy and Area Efficient Near Field Inductive Coupling: A Case study on 3D NoC

Authors: Srinivasan Gopal, Sourav Das, Deukhyon Heo and Partha Pande (Washington State Univ.)

*50 Achieving Lightweight Multicast in Asynchronous NoCs Using a Continuous-Time Multi-Way Read Buffer

Authors: Kshitij Bhardwaj, Weiwei Jiang and Steven M. Nowick (Columbia Univ.)

*65 BiNoCHS: Bimodal Network-on-Chip for CPU-GPU Heterogeneous Systems

Authors: Amirhossein Mirhosseini (Univ. of Michigan), Mohammad Sadrosadati, Behnaz Soltani, Hamid Sarbazi-Azad (Sharif Univ. of Technology) and Thomas Wenisch (Univ. of Michigan)

[15:00 – 15:30] Coffee Break

[15:30 – 17:30] Panel: Networks-on-Chip: Past, Present and Future

Moderator: Axel Jantsch (TU Wien)

Panelists:

- Luca Carloni (Columbia Univ., USA)
- Ahmed Hemani (KTH Royal Institute of Technology, Sweden)
- Nanni de Micheli (EPFL, Switzerland)
- Vijaykrishnan Narayanan (Pennsylvania State Univ., USA)
- Partha Pande (Washington State Univ., USA)
- Sudhakar Yalamanchili (Georgia Tech., USA)

[19:00] NOCS Banquet

NOCS 2017 Program (cont.)

FRIDAY OCT 20, 2017

[07:30-08:30] Breakfast

[08:30 – 10:00] Special session 1:"Driving Networks from Chips to Vehicles"

Session chair: Zhonghai Lu (KTH Royal Institute of Technology)

Addressing Extensibility and Fault Tolerance in CAN-based Automotive Systems

Authors: Hengyi Liang, Zhilu Wang, Bowen Zheng, Qi Zhu (University of California, Riverside)

JAMS: Jitter-aware Message Scheduling for FlexRay Automotive Networks

Authors: Vipin Kumar Kukkala, Sudeep Pasricha (Organizer), Thomas Bradley (Colorado State University)

Hybrid Automotive In-Vehicle Networks

Authors: Debayan Roy, Michael Balszun, Dip Goswami, Samarjit Chakraborty (TU Eindhoven)

[10:00 – 10:30] Coffee Break

[10:30 – 12:30] Session 3: "QoS and Application Mapping"

Session chair: Ahmed Hemani (KTH Royal Institute o f Technology)

23 Fairness-Oriented and Location-Aware NUCA for Many-Core SoC

Authors: Zicong Wang, Xiaowen Chen, Chen Li and Yang Guo (National Univ. of Defense Technology)

40 On the Accuracy of Stochastic Delay Bound for Network on Chip

Authors: Gaoming Du, Yongliang Zhang, Guanyu Liu, Zhenmin Li, Duoli Zhang and Yiming Ouyang (Hefei Univ. of Technology)

10 SMART: A Scalable Mapping And Routing Technique for Power-Gating in NoC Routers

Authors: Hossein Farrokhbakht, Hadi Mardani Kamali and Shaahin Hessabi (Sharif Univ. of Technology)

7 On Runtime Communication- and Thermal-aware Application Mapping in 3D NoC

Authors: Bing Li, Xiaohang Wang (South China Univ. of Technology), Amit Kumar Singh (Univ. of Southampton) and Terrence Mak (Univ. of Southampton)

[12:30 – 13:30] Lunch Break

[13:30 – 15:00] Session 4: NoC design for 3D stacking and neural networks

Session chair: Vassos Soteriou (Cyprus University of Technology)

32 XYZ-Randomization using TSVs for Low-Latency Energy-Efficient 3D-NoCs

Authors: Hiroshi Nakahara, Nguyen Anh Vu Doan, Ryota Yasudo and HIDEHARU AMANO (Keio Univ.)

53 3D NoC-Enabled Heterogeneous Manycore Architectures for Accelerating CNN Training: Performance and Thermal Trade-offs

Authors: Biresh Joardar, Wonje Choi (Washington State Univ.), Ryan Kim (Carnegie Mellon Univ.), Jana Doppa, Partha Pande (Washington State Univ.), Diana Marculescu and Radu Marculescu (Carnegie Mellon Univ.)

12 Rethinking NoCs for Spatial Neural Network Accelerators

Authors: Hyoukjun Kwon, Ananda Samajdar and Tushar Krishna (Georgia Institute of Technology)

[15:00 – 15:30] Coffee Break

[15:30 – 16:50] Special Session 2: Adaptive Manycore Architectures for Big Data Computing

Session chair: Partha Pande (Washington State University)

Adaptive Manycore Architectures for Big Data Computing

Contributors:

- Janardhan Rao Doppa (Washington State Univ.)
- Ryan Kim (Carnegie Mellon Univ.)
- Mihailo Isakov and Michel A. Kinsy (Boston Univ.)
- HyoukJun Kwon and Tushar Krishna (Georgia Institute of Technology)

[16:50 – 17:00] Closing Remark

THURSDAY OCT 19, 2017

Symposia - The International Symposium on Rapid System Prototyping (RSP)

Time: 08:30 - 17:00 | Room: Berkely, 36F

The International Symposium on Rapid System Prototyping (RSP) emphasizes design experience sharing and collaborative approach between hardware and software research communities from industry and academy. It considers prototyping as an iterative design approach for embedded hardware and software systems. The RSP series of symposium aim at bridging the gaps in embedded system design between applications, architectures, tools, and technologies to achieve rapid system prototyping of emerging software and hardware systems.

SCHEDULE:

Thursday - 08:30am to 17:00

Friday - 08:30am to 12:30

2017 General Chairs

Fabiano Hessel, *Pontifical Catholic Univ. of Rio Grande do Sul*

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Sungjoo Yoo, *Seoul National Univ.*

[08:30 - 10:00] Session 1:

Session Chair: Frederic Rousseau - *TIMA, Univ. Grenoble-Alpes*

8:30 - Opening remarks

8:45 - Chanik Park (VP Samsung Electronics), "Storage Technology Trends for Data-Centric Applications"

[10:00 – 10:30] Coffee Break

[10:30 - 12:30] Session 2:

Session Chair: Sungjoo Yoo - *Seoul National Univ.*

10:30 - (Invited Paper) Saideep Tiku and Sudeep Pasricha, "Energy-Efficient and Robust Middleware Prototyping for Smart Mobile Computing"

11:00 - Michael Witterauf, Frank Hannig and Jürgen Teich, "Constructing Fast and Cycle-Accurate Simulators for Configurable Accelerators Using C++ Templates"

11:30 - Arief Wicaksana, Alban Bourge, Olivier Muller, Arif Sasongko and Frédéric Rousseau, "Prototyping Dynamic Task Migration on Heterogeneous Reconfigurable Systems"

12:00 - Tiago Rogério Mück, Bryan Donyanavard and Nikil Dutt, "PoliCym: Rapid prototyping of resource management policies for HMPs"

[12:30 – 13:30] Lunch Break

[13:30 – 15:00] Session 3:

Session Chair: Kyoungwoo Lee - *Yonsei Univ.*

13:30 - (Invited Paper) Wooseok Yi, Junki Park, and Jae-Joon Kim, "GeCo: Classification Restricted Boltzmann Machine Hardware for On-chip Learning"

14:00 - Sean Seeley, Vidya Sankaranaryanan, Zack Deveau, Panagiotis Patros and Kenneth Kent, "Simulation-Based Circuit-Activity Estimation for FPGAs Containing Hard Blocks"

14:30 - Maha Kooli, Henri-Pierre Charles, Clément Touzet, Bastien Giraud and Jean-Philippe Noel, "Software Platform Dedicated for In-Memory Computing Circuit Evaluation"

14:45 - Jeonggyu Jang and Hoeseok Yang, "Executable Dataflow Benchmark Generation Technique for Multi-Core Embedded Systems"

[15:00 – 15:30] Coffee Break

[15:30 - 17:00] Session 4:

Session Chair: Panagiotis Patros - *Univ. of New Brunswick*

15:30 - Peter Volgyesi, Abhishek Dubey, Timothy Krentz, Istvan Madari, Mary Metelko and Gabor Karsai, "Time Synchronization Services for Low-cost Fog Computing Applications"

16:00 - Imane Hafnaoui, Chao Chen, Rabeh Ayari, Gabriela Nicolescu and Giovanni Beltrame, "An Analysis of Random Cache Effects on Real-Time Multi-core Scheduling Algorithms"

16:30 - Minato Yokota, Kaoru Saso and Yuko Hara-Azumi, "One-Instruction Set Computer-based Multicore Processors for Energy-Efficient Streaming Data Processing"

FRIDAY OCT 20, 2017

[08:30 - 10:00] Session 5:
Joint Session with HENND 2017

08:30 - Prof Yoshua Bengio (Univ. of Montreal), "Towards End-to-End Trainable Hardware"

09:20 - Prof Hoi-Jun Yoo (KAIST), "Mobile/Embedded Neural Networks and Applications"

[10:00 – 10:30] Coffee Break

[10:30 - 12:30] Session 6:
Session Chair: Hoeseok Yang - *Ajou Univ.*

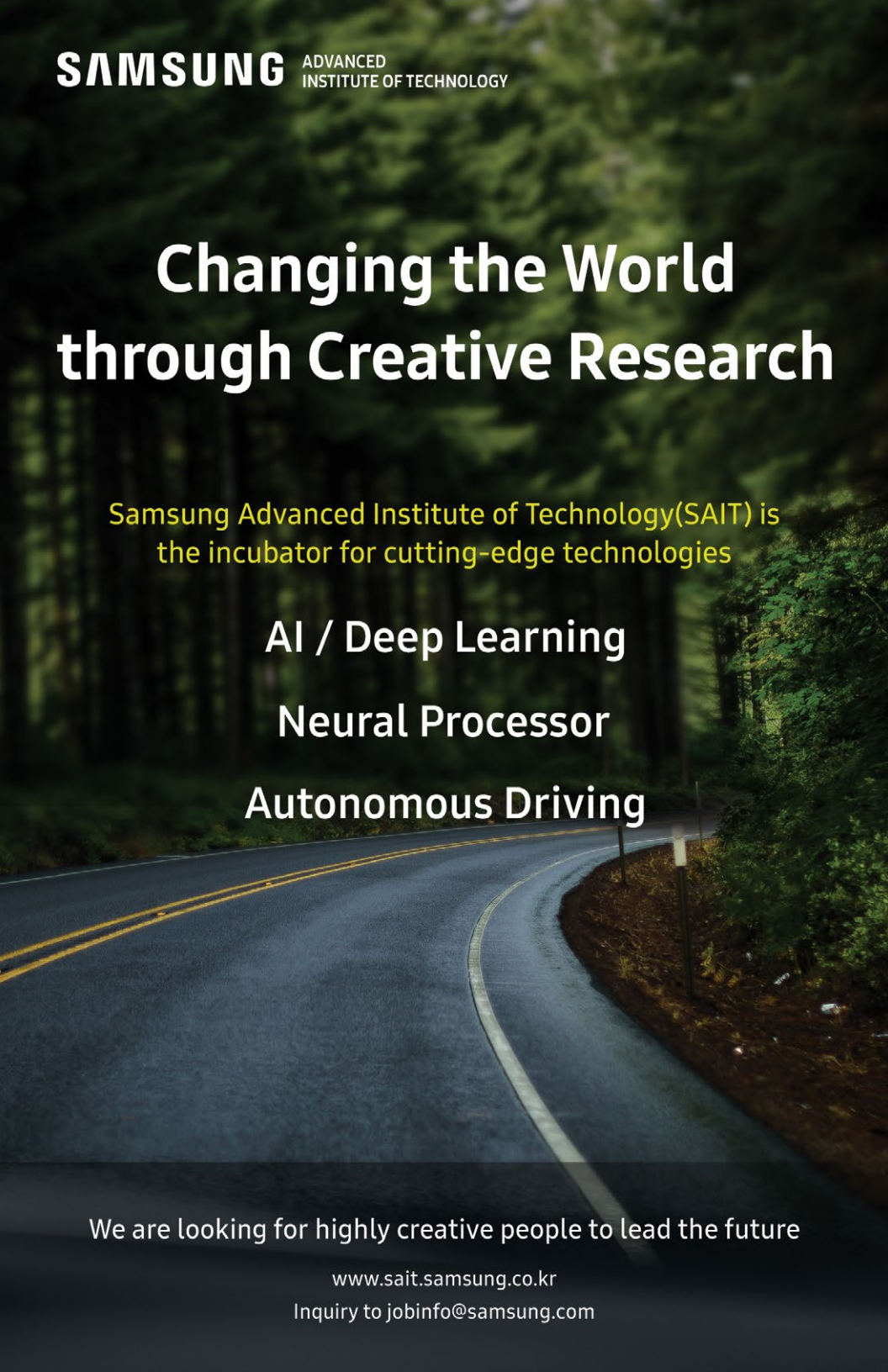
10:30 - (Invited Paper) Daniel Mueller-Gritschneder, Martin Diettrich, Marc Greim, Keerthikumara Devarajegowda, Wolfgang Ecker and Ulf Schlichtmann,"The Extendable Translating Instruction Set Simulator (ETISS) interlined with a Code Generation Framework for Fast RISC Prototyping"

11:00 - (Invited Paper) Gyeongmin Lee, Seonyeong Heo, Bongjun Kim, Jong Kim, and Hanjun Kim, "Rapid prototyping of IoT applications with Esperanto compiler"

11:30 - Naoya Ito, Yuuki Oosako, Nagisa Ishiura, Hiroyuki Tomiyama and Hiroyuki Kanbara, "Binary Synthesis Implementing External Interrupt Handler as Independent Module"

12:00 - Miho Shimizu, Nagisa Ishiura, Sayuri Ota and Wakako Nakano, "Speculative Execution in Distributed Controllers for High-Level Synthesis"

[12:30 – 13:30] Lunch Break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One Registration, three Conferences !

Registered attendees are entitled to attend sessions of all conferences CASES, CODES+ISSS, EMSOFT, and the IoT Day. Symposia, workshops and tutorials require separate registration.

Journal Track:
Abstract Submission: March 31, 2017
Full Paper Submission: April 7, 2017 (firm)
Notification of Acceptance: June 30, 2017

Work-in-Progress Track:
Paper Submission: June 2, 2017 (firm)
Notification of Acceptance: June 30, 2017

Workshop Proposals: March 10, 2017
Tutorial Proposals: April 7, 2017

CASES — International Conference on Compilers, Architectures, and Synthesis for Embedded Systems

CASES is a premier forum where researchers, developers and practitioners exchange information on the latest advances in compilers and architectures for high-performance, low-power embedded systems. The conference has a long tradition of showcasing leading edge research in embedded processor, memory, interconnect, storage architectures and related compiler techniques targeting performance, power, predictability, security, reliability issues for both traditional and emerging application domains. In addition, we invite innovative papers that address design, synthesis, and optimization challenges in heterogeneous and accelerator-rich architectures.

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IoT — Internet-of-Things

The Internet of Things (IoT) promises to revolutionize fields ranging from health care to manufacturing to personal living by connecting the Internet to physical things. Embedded computing is central to the achievement of the IoT vision – advanced computation, communication, and storage must be delivered in a safe, secure, and reliable manner at extremely low energy levels. The IoT special day is devoted to research on advanced IoT systems. It will provide a forum for academia and industry to present and discuss innovative ideas and solutions related to all facets of internet-of-things. Submissions to the IoT day are done via the three conferences.

IoT Chair
Prabal Dutta, University of Michigan, US

ESWEEK 2017 introduces a dual publication model with two tracks: Journal track papers will be published in ACM Transactions on Embedded Computing Systems, and Work-in-Progress track papers will be published in the ESWEEK Proceedings.
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