EMBEDDED SYSTEMS WEEK

CASES 2017

CASES

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Call for Papers

International Conference on
Compilers, Architectures, and Synthesis for Embedded Systems
October 15-20, 2017, Seoul, South Korea

CASES is a premier forum where researchers, developers and practitioners exchange information on the latest advances in compilers and architectures for high-performance, low-power embedded systems. The conference has a long tradition of showcasing leading edge research in embedded processor, memory, interconnect, storage architectures and related compiler techniques targeting performance, power, predictability, security, reliability issues for both traditional and emerging application domains. We also invite innovative papers addressing design, synthesis & optimization challenges in heterogeneous, accelerator-rich architectures.

Abstract Submission:
March 31, 2017

Full Paper Submission:
April 7, 2017 (firm deadline)

Work-in-Progress Papers:
June 2, 2017 (firm deadline)

Conference:
October 15-20, 2017

Processor Architectures: Multi- and many-core processors, Embedded and mobile processor micro-architecture, GPU architectures, Reconfigurable computing including FPGAs and CGRAs, Application-Specific processor design, 3D-stacked architectures.

Memory and Storage: Memory system architecture; Non-volatile and other emerging memory technologies; Scratchpad memory, caches and compiler controlled memories; storage organization including flash storage.

On-chip communication and I/O: Networks-on-chip architectures and design methodologies; on-chip communication synthesis, analysis, and optimization; I/O management in embedded systems.

Compilers for Embedded Systems: Compilation for power and performance; Compiler support for GPUs, FPGAs, CGRAs, heterogeneous multi-core SoC; compilation for memory, storage, and on-chip communications.

Power and Thermal: Power- and energy-efficient architectures; Compilation and runtime management for low-power and thermally-constrained embedded systems.

Security, Reliability, and Predictability: Secure architectures, hardware security, and compilation for software security; Architecture and compiler techniques for reliability and aging; Modeling, design, analysis, and optimization for timing and predictability; Validation, verification, testing & debugging of embedded software.

Emerging Application Domains and Accelerators: Synthesis of accelerators for machine learning, neuromorphic & cognitive computing, data analytics; Architectures, compiler & synthesis for emerging nanoscale devices, biologically inspired computing systems, programmable microfluidics & synthetic biology; Architectures, compilers & synthesis for approximate computing.

Internet of Things (IoT) Day: A specal IoT Day will be jointly organized by all conferences in ESWeek. Topics for CASES include: Architecture, compiler, and synthesis for IoT platforms, wearables and other small form-factor devices; Low-power, high-performance and reliable design of micro-controllers, accelerators and SoCs for edge computing and gateways; Compiler for ultra-low power IoT applications; Secure software development, secure hardware design and synthesis for IoT.

CASES will follow double-blind two-stage review process, where papers passing the first-stage of reviews may be asked to submit a revised version within a timeframe of about three weeks for a second-stage of reviews.
See http://www.esweek.org/author-information for details.

Journal-integrated Publication Model: ESWEEK 2017 will introduce a journal-integrated publication model where the majority of papers will be published in the ACM Transactions on Embedded Computing Systems (TECS).

ESWeek General Chairs:
Lothar Thiele, Swiss Federal Institute of Technology, CH
Soonhoi Ha, Seoul National University, KR

CASES Program Chairs:
Laura Pozzi, USI University of Lugano, CH
Tulika Mitra, National University of Singapore, SG