CODES+ISSS 2017

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Call for Papers

International Conference on Hardware/Software Codesign and System Synthesis
October 15-20, Lotte Hotel, Seoul, South Korea

The International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) is the premier event in system-level design, modeling, analysis, and implementation of modern embedded and cyber-physical systems, from system-level specification and optimization down to system synthesis of multi-processor hardware/software implementations. The conference is a forum bringing together academic research and industrial practice for all aspects related to system-level and hardware/software co-design. CODES+ISSS 2017 is part of the Embedded Systems Week (ESWeek) 2017.

Journal-track abstract submission:
March 31, 2017

Journal-track paper submission:
April 7, 2017 (Firm deadline)

First journal-track paper notification:
May 21, 2017

WiP paper submission:
Friday, June 2 (Firm deadline)

Revised journal paper submission:
June 11, 2017

Notification of acceptance:
June 30, 2017

Camera-ready version:
July 14, 2017

CODES+ISSS invites contributions on specification, modelling, design, analysis, and implementation of embedded and cyber-physical systems. The following relevant areas are representative but not exhaustive. We welcome submissions on novel solutions, new challenges, and emerging technologies in all these areas. This year, we particularly invite IoT-related submissions that will be presented during ESWeek's Special Day on IoT.

Track 1) System-level design – Specification, modelling, refinement, system synthesis, partitioning, hardware-software co-design, design space exploration, hybrid system modelling and design, model-based design, and design for adaptivity and reconfigurability.

Track 2) Domain and application-specific design- Analysis, design, and optimization techniques for multimedia, medical, automotive, cyber-physical, and other specialized application domains.

Track 3) Embedded software - Language and library support, compilers, runtimes, parallelization, software verification, memory management, virtual machines, operating systems, real-time support, and middleware.

Track 4) Security and reliability – Cross-layer reliability, resilience and fault tolerance, test methodology, design for testability, hardware and software security, and cyber-physical system security.

Track 5) Simulation, validation and verification - Hardware/software co-simulation, verification and validation methodologies, formal verification, hardware-accelerated simulation, simulation and verification languages, models and benchmarks.

Track 6) System architecture - Heterogeneous systems, many-cores, networked and distributed systems. architecture and micro-architecture design, exploration and optimization including application-specific processors, reconfigurable architectures, storage, memory and communication systems, and networks-on-chip.

Track 7) Power-efficient systems - Power- and energy-aware system design and methodologies ranging from low-power embedded and cyber-physical systems to energy-efficient large scale systems such as Green IT and Smart Grid.

Track 8) Industrial practices and case studies - Practical impact on current and/or future industries, application of state-of-the-art methodologies and tools in various application areas including wireless, networking, multimedia, automotive, cyber-physical, medical systems, etc.

ESWeek 2017 features a dual publication model with full-length *Journal-track papers* (published in ACM TECS) and short (2-page) *Work-in-Progress (WiP) track papers* (published in the ESWEEK proceedings): see http://www.esweek.org/

ESWeek General Chairs:
Lothar Thiele, Swiss Federal Institute of Technology, CH
Soonhoi Ha, Seoul National University, KR

CODES+ISSS Program Chairs:
Andy Pimentel, University of Amsterdam, NL
Aviral Shrivastava, Arizona State University, US

http://www.esweek.org/codesisss