EMBEDDED SYSTEMS WEEK

15TH ACM/IEEE EMBEDDED SYSTEMS WEEK

2019 ESWEEK PROGRAM

OCTOBER 13 - 18, 2019 | NEW YORK CITY, NY | USA

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WELCOME TO ESWEEK 2019

Petru Eles | General Chair
Linköping Univ., SE

Tulika Mitra | Vice-General Chair
National Univ. of Singapore, SG

Welcome to ESWEEK 2019 in New York City!

Embedded Systems Week (ESWEEK) is the premier event covering all aspects of embedded systems and software. By bringing together three leading conferences (CASES, CODES+ISSS, EMSOFT), a special day on IoMT (Internet of Medical Things), one symposium (NOCS), and hot-topic workshops, special sessions, and tutorials, ESWEEK presents attendees a wide range of choices unveiling state of the art embedded systems design and hardware/software architectures.

Following the journal-integrated publication model for the three conferences (CASES, CODES+ISSS, and EMSOFT), all regular papers presented are published in the ACM Transactions on Embedded Computing Systems. To this end, the review process of the conferences was conducted in two stages with the opportunity of minor/major revisions before the final decision. In addition, the selected Work-in-Progress track papers are published in the ESWEEK Proceedings.

The technical program on Monday, Tuesday, and Wednesday consists of six special sessions and 25 regular sessions from the three conferences. There is a strong emphasis on interaction as, connected to each paper, there also is a poster presentation during which the participants can discuss the papers with the authors.

On Tuesday we have the special IoMT day, focusing on the newest developments in the "Internet of Medical Things" from an embedded and cyber-physical systems perspective. A sequence of three special sessions is exclusively devoted to this subject.

Highlights of the ESWEEK program are three distinguished keynote talks by prominent leaders in academia and industry, covering most relevant trends for future embedded and cyber-physical systems and providing deep insights into technology drivers. Dr. Stephen Keckler, Vice President of Architecture Research at NVIDIA and Adjunct Professor at the University of Texas at Austin, addresses the impact of modern applications with huge computational requirements such as intelligent video analytics, autonomous vehicles, and robotics on the world of embedded computing devices. Professor Dina Katabi, from MIT, will introduce Emerald, a new wireless technology that uses machine learning for health monitoring at home without the requirement to wear any sensors or wearables. By monitoring a variety of physiological signals continuously and without imposing a burden on users, Emerald can automatically detect degradation in health, enabling early intervention and care. In his Wednesday keynote, Professor Pramod Khargonekar, Vice Chancellor for Research, University of California Irvine, argues that by meaningfully connecting the field of cyber-physical systems with machine learning on the one hand and social-behavioral-economic sciences on the other, future research can make contributions of huge significance to the society.

The conference program will conclude with the traditional panel on Wednesday afternoon focusing on "The Internet of Medical Things (IoMT): What is the Future?" Top experts from academia and industry will share their views on this highly relevant topic.

The tutorials on Sunday precede the conferences and are an excellent opportunity to get in-depth knowledge in new trends and hot topics. There are six half-day tutorials and one full-day tutorial, covering a wide scope, from machine learning security to open-source hypervisors for embedded platforms. Two of the tutorials are offered by industry sponsors Intel and Xilinx.

Thursday and Friday are the days for the symposium and workshops. Besides the NOCS (Networks on Chip) symposium, we have seven workshops covering a wide range of important topics in embedded systems: RSP (Rapid System Prototyping), AAIEA (Accelerating Artificial Intelligence for Embedded Autonomy), CyberCardia (Medical CPS Systems), EWiLi (Embedded Operating Systems), HENP (Highly Efficient Neural Processing), INTESA (INTelligent Embedded Systems Architecture and Applications), and a merger of CyPhy (Model-Based Design of Cyber Physical Systems) with WESE (Workshop on Embedded Systems Education).

The organization of ESWEEK was only possible with the continuous support and help from many volunteers: The program chairs with their program committee members, the organizers of the special day, the workshops, tutorials, and symposia, all members of the organization committee, and, last but not least, the local arrangements chairs and their team.

We are looking forward to meeting you at the inspiring and interesting ESWEEK 2019 in New York City!

GENERAL INFORMATION

Welcome to New York!

The City of New York, usually called either New York City (NYC) or simply New York (NY), is the most populous city in the United States. A global power city, New York City has been described as the cultural, financial, and media capital of the world,and exerts a significant impact upon commerce, entertainment, research, technology, education, politics, tourism, art, fashion, and sports. Several sources have ranked New York the most photographed city in the world. Times Square, iconic as the world's "heart" and its "Crossroads", is the brightly illuminated hub of the Broadway Theater District, one of the world's busiest pedestrian intersections, and a major center of the world's entertainment industry. The names of many of the city's landmarks, skyscrapers, and parks are known around the world.

New York City is a tourist's paradise and has witnessed a growing combined volume of international and domestic tourists, receiving approximately 62.8 million visitors in 2017. Major tourist destinations include Times Square; Broadway theater productions; the Empire State Building; the Statue of Liberty; Ellis Island; the United Nations Headquarters; museums such as the Metropolitan Museum of Art; greenspaces such as Central Park and Washington Square Park (the main venue for ESWeek 2019); Rockefeller Center; the Manhattan Chinatown; luxury shopping along Fifth and Madison Avenues; and events such as the Halloween Parade in Greenwich Village; the Macy's Thanksgiving Day Parade; the lighting of the Rockefeller Center Christmas Tree; the St. Patrick's Day parade; seasonal activities such as ice skating in Central Park in the wintertime; the Tribeca Film Festival; and free performances in Central Park at Summerstage. Major attractions in the boroughs outside Manhattan include Flushing Meadows-Corona Park and the Unisphere in Queens; the Bronx Zoo; Coney Island, Brooklyn; and the New York Botanical Garden in the Bronx. Embedded Systems Week will be held at New York University's campuses in New York City. The main conference events are at NYU's Manhattan campus, around the picturesque Washington Square Park in Greenwich Village, one of New York City's most historic neighborhoods, known as an artists' haven, its Bohemian capital, the cradle of the modern LGBT movement, and the East Coast birthplace of both the Beat and '60s counterculture movements. Then, for the workshops, we move across the iconic Brooklyn Bridge to NYU's engineering campus in trendy Brooklyn, a thriving hub of entrepreneurship and high technology startup firms, of postmodern art and design. We encourage ESWeek attendees to enjoy, explore and take advantage of the City that Never Sleeps!

[Source: Wikipedia]

ESWEEK 2019 OVERVIEW

Sunday, October 13

Tutorials

Welcome Reception

Monday, October 14

Opening Session

Keynote by Steve Keckler

CASES, CODES+ISSS, & EMSOFT Sessions

Poster Sessions

ACM Student Research Competition

Technical Program Committee Dinner

Tuesday, October 15

Keynote by Dina Katabi

CASES, CODES+ISSS, EMSOFT & IoMT Day Sessions

Poster Sessions

IoMT Design Contest

Social Event - Carmine's Restaurant in Times Sq & Broadway Show

Wednesday, October 16

Keynote by Pramod Khargonekar

CASES, CODES+ISSS, EMSOFT Sessions

Poster Sessions

ACM Student Research Competition

Awards Ceremony

ESWEEK Panel

Thursday, October 17

NOCS Symposium

AAIEA Workshop

CyberCardia Workshop

CyPhy/WESE Workshop

EWiLi Workshop

HENP Workshop

INTESA Workshop

RSP Wokshop

Friday, October 18

NOCS Symposium

CyPhy/WESE Workshop

RSP Workshop

CONFERENCE VENUE

Conference Venue at a Glance

Event	Days	Venue	Building/Address	Travel
ESWeek Tutorials	Sunday	NYU Washington Square Campus (See Map A)	**Furman Hall** 245 Sullivan St, New York, NY 10012	Closest subway is West 4th St. subway in Manhattan, served by A, C, E, B, D, F, M
ESWeek Sunday Reception	Sunday		**NYU AD Building** 19 Washington Square North New York, NY 10011	
ESWeek Main Conference	Mon.-Wed.		**Kimmel Center (KC)** 60 Washington Square S, New York, NY 10012	
Networks on Chip Symposium (NOCS)	Thu.-Fri.		**NYU AD Building** 19 Washington Square North New York, NY 10011	
ESWeek Workshops	Thu.-Fri.	NYU Brooklyn Campus (See Map B)	**370 Jay St.** 370 Jay St. Brooklyn, NY 11201	Closest subway is Jay St. Metrotech subway in Brooklyn, served by A, C, F

Directions from NYU Washington Square to NYU Brooklyn:

The fastest way is via subway. From the West 4th St. Subway Stations (see Map A), take A,C,F towards Downtown/ Brooklyn and get off at the Jay St. Subway Station. The travel time is roughly 20 minutes and costs $2.75.

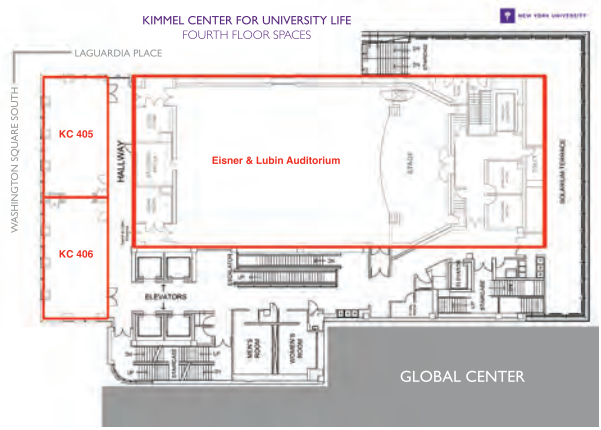
Map A: NYU Washington Square Campus

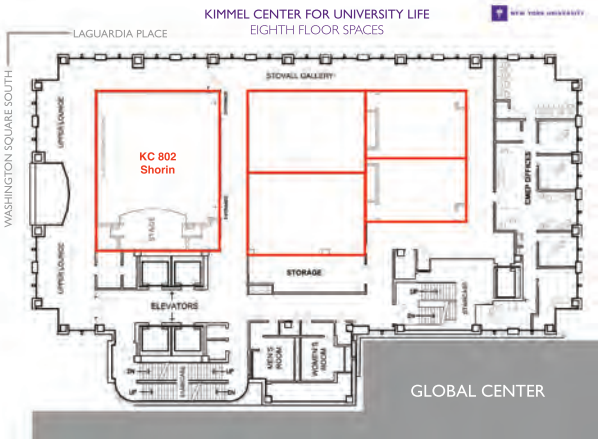
Map B: NYU Brooklyn Campus

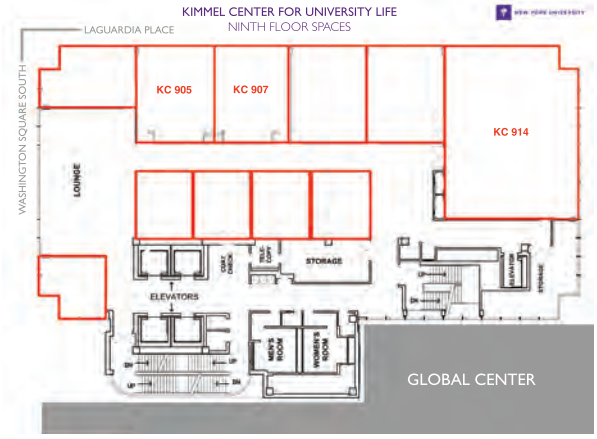
CONFERENCE VENUE

Kimmel Center (KC) Floorplans

The ESWeek Main Conference will be held in Kimmel Center (KC) and spread out over three floors: Floors 4, 8 and 9. Floorplans of these floors are below.







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BEST PAPER CANDIDATES

CASES

1A.2 AGGRESSIVE ENERGY REDUCTION FOR VIDEO INFERENCE WITH SOFTWARE-ONLY STRATEGIES

Authors:

Larissa Rozales Gonçalves - *Univ. Federal do Rio Grande do Sul*
Rafael Fão de Moura -*Univ. Federal do Rio Grande do Sul*
Luigi Carro - *Univ. Federal do Rio Grande do Sul*

2A.2 AN ULTRA-LOW ENERGY HUMAN ACTIVITY RECOGNITION ACCELERATOR FOR WEARABLE HEALTH APPLICATIONS

Authors:

Ganapati Bhat - *Arizona State Univ.*
Yigit Tuncel - *Arizona State Univ.*
Sizhe An - *Arizona State Univ.*
Hyung Gyu Lee - *Daegu Univ., Republic of Korea*
Umit Ogras - *Arizona State Univ.*

6A.1 OUTPUT-BASED INTERMEDIATE REPRESENTATION FOR TRANSLATION OF TEST PATTERN PROGRAMS

Authors:

Minsu Kim - *Seoul National Univ., Republic of Korea*
Jeong-keun Park - *Seoul National Univ., Republic of Korea*
Sungyeol Kim - *Samsung Electronics Co., Ltd*
Insu Yang - *Samsung Electronics Co., Ltd*
Hyunsoo Jung - *Samsung Electronics Co., Ltd*
Soo-Mook Moon - *Seoul National Univ., Republic of Korea*

CODES + ISSS

3B.1 ACHIEVING SUPER-LINEAR SPEEDUP ACROSS MULTI-FPGA FOR REAL-TIME DNN INFERENCE

Authors:

Weiwen Jiang - *Univ. of Pittsburgh*
Edwin Sha - *East China Normal Univ.*
Xinyi Zhang - *Univ. of Pittsburgh*
Lei Yang - *Chongqing Univ., China*
Qingfeng Zhuge - *East China Normal Univ.*
Yiyu Shi - *Univ. of Notre Dame*
Jingtong Hu - *Univ. of Pittsburgh*

3B.2 ACHIEVING LOSSLESS ACCURACY WITH LOSSY PROGRAMMING FOR EFFICIENT NEURAL-NETWORK TRAINING ON NVM-BASED SYSTEMS

Authors:

Wei-Chen Wang - *Macronix International Co., Ltd., Taiwan*
Yuan-Hao Chang - *Academia Sinica, Taiwan*
Tei-Wei Kuo - *National Taiwan Univ.*
Chien-Chung Ho - *National Chung Cheng Univ., Taiwan*
Yu-Ming Chang - *National Taiwan Univ., Taiwan*
Hung-Sheng Chang - *Macronix International Co., Ltd.*

5B.1 ACCUMULATIVE DISPLAY UPDATING FOR INTERMITTENT SYSTEMS

Authors:

Hashan Roshantha Mendis - *Academia Sinica, Taiwan*
Pi-Cheng Hsiu - *Academia Sinica, Taiwan*

EMSOFT

1C.1 DERIVING EQUATIONS FROM SENSOR DATA USING DIMENSIONAL FUNCTION SYNTHESIS

Authors:

Sam Willis - *Cambridge Univ.*
Youchao Wang - *Cambridge Univ.*
Vasileios Tsoutsouras - *Cambridge Univ.*
Phillip Stanley-Marbell - *MIT*

4C.1 STATISTICAL VERIFICATION OF HYPERPROPERTIES FOR CYBER-PHYSICAL SYSTEMS

Authors:

Yu Wang - *Duke Univ.*
Mojtaba Zarei - *Duke Univ.*
Borzoo Bonakdarpour - *Iowa State Univ.*
Miroslav Pajic - *Duke Univ.*

4C.2 POLAR: FUNCTION CODE AWARE FUZZ TESTING OF ICS PROTOCOL

Authors:

Zhengxiong Luo - *Tsinghua Univ.*
Feilong Zuo - *Tsinghua Univ.*
Yu Jiang - *Tsinghua Univ.*
Jian Gao - *Tsinghua Univ.*
Xun Jiao - *Villanova Univ.*
Jiaguang Sun - *Tsinghua Univ.*

SUNDAY, OCTOBER 13
TUTORIALS SCHEDULE

	Furman Hall 120	Furman Hall 214	Furman Hall 210	Furman Hall 212
09:00 - 18:00	Hardware Design in the 21st Century with the Object Oriented and Functional Language Chisel	Machine Learning for Design and Optimization of Embedded Systems	Machine Learning Security	Industry Tutorial: The Open Source ACRN Hypervisor on an Intel Embedded Platform
09:00 - 13:00				
13:00 - 14:00	Lunch | Room: NYU AD			
14:00 - 18:00	Hardware Design in the 21st Century with the Object Oriented and Functional Language Chisel	Open-Source Hardware: Heterogeneous System Integration with Embedded Scalable Platforms	HW/SW Modeling and Performance Analysis of Heterogeneous Safety-Critical Systems	Industry Tutorial: PYNQ: Python Productivity for Zynq
18:00 - 20:00	Welcome Reception | Room: NYU AD Building			

Tutorial 1 - Hardware Design in the 21st Century with the Object Oriented and Functional Language Chisel

Time: 9:00 - 18:00 | Room: Furman Hall 120

Organizer:

Martin Schoeberl - *Technical Univ. of Denmark*

Speakers:

Martin Schoeberl - *Technical Univ. of Denmark*
Schuyler Eldridge - *IBM T. J. Watson Research Center*

To develop future more complex digital circuits in less time we need a better hardware description language than VHDL or Verilog. Chisel is a hardware construction language intended to speedup the development of digital hardware and hardware generators.

Chisel is a hardware construction language implemented as a domain specific language in Scala. Therefore, the full power of a modern programming language is available to describe hardware and, more important, hardware generators. Chisel has been developed at UC Berkeley and successfully used for several tape outs of RISC-V by UC Berkeley students and a chip for a tensor processing unit by Google. Here at the Technical Univ. of Denmark we use Chisel in the T-CREST project and in teaching advanced computer architecture.

The Chisel/FIRRTL Hardware Compiler Framework enables back end specialization (e.g., to target specific FPGAs or ASIC technologies) and LLVM-like programmability via use of existing transforms (e.g., for run-time fault injection) or user-defined custom transformations. The tutorial will include an overview of the architecture of the Chisel/FIRRTL Hardware Compiler Framework and the design and use of custom FIRRTL transformations to automate the low-level modification of FIRRTL circuits.

The tutorial consists of two sessions. In the morning session. we will give an overview of Chisel to describe circuits, how to use the Chisel tester functionality to test and simulate digital circuits, and present how to synthesize circuits for an FPGA.

The advanced functionality of Chisel for the description of circuit generators, including concepts of circuit generators and background of the hardware representation in FIRRTL will be presented in the afternoon session. Therefore, for just a brief introduction to Chisel the second session is optional.

The aim of the course is to get a basic understanding of a modern hardware description language and be able to describe simple circuits in Chisel. This course will give a basis to explore more advanced concepts of circuit generators written in Chisel/Scala. The intended audience is hardware designers with some background in VHDL or Verilog, but Chisel is also a good first hardware language for software programmers entering into hardware design (e.g., porting software algorithms to FPGAs for speedup).

BIOGRAPHIE(S):

Martin Schoeberl received his PhD from the Vienna Univ. of Technology in 2005. From 2005 to 2010 he has been Assistant Professor at the Institute of Computer Engineering. He is now Associate Professor at the Technical Univ. of Denmark. His research interest is on hard real-time systems, time-predictable computer architecture, and real-time Java. Martin Schoeberl has been involved in a number of national and international research projects: JEOPARD, CJ4ES, T-CREST, RTEMP, the TACLe COST action, and PREDICT. He has been the technical lead of the EC funded project T-CREST. He has more than 100 publications in peer reviewed journals, conferences, and books. Martin has been four times at UC Berkeley on 3-4 months research stays, where he has picked up Chisel and was in close contact with the developers of Chisel. He lead the research project T-CREST where most of the components have been written in Chisel. Martin is currently finalizing the book ``Digital Design with Chisel'', which is available in open source. The first edition of the Chisel book will be available at the tutorial.

Schuyler Eldridge received his PhD from Boston Univ. in 2016 where he worked to build machine learning accelerators and hardware monitors integrated with the RISC-V Rocket Chip project. He joined IBM T. J. Watson in 2016 and is currently a research staff member there working in the Reliability and Power-Aware Microarchitectures group. He has been involved with the DARPA PERFECT and DSSoC programs working to rapidly build SoCs, develop/integrate accelerator hardware, and improve hardware design methodologies through the application of software engineering paradigms. Schuyler is an active contributor to and code reviewer on the Chisel and FIRRTL projects. Most recently he has contributed the BoringUtils API to Chisel and led the "Stage/Phase" refactor of Chisel and FIRRTL. He is also the author of DANA, a machine learning accelerator in

Chisel, and the Chiffre Chisel/FIRRTL run-time fault injection framework.

Tutorial 2 - Open-Source Hardware: Heterogeneous System Integration with Embedded Scalable Platforms

Time: 14:00 - 18:00 | Room: Furman Hall 214

Organizer:

Luca P. Carloni - *Columbia Univ.*

Speakers:

Luca P. Carloni - *Columbia Univ.*
Giuseppe Di Guglielmo - *Columbia Univ.*
Davide Giri - *Columbia Univ.*
Paolo Mantovani - *Columbia Univ.*

Heterogeneous systems-on-chip empower all modern intelligent systems. We start by explaining the implications of the ever-increasing variety of specialized accelerators present in SoCs: the price for the efficiency gain they offer is the complexity of system integration. To address this challenge, we developed Embedded Scalable Platforms. By combining a scalable architecture with a system-level methodology, ESP simplifies the design of individual accelerators and automates their hardware/software integration. First, we discuss the properties of ESP that are key for open-source hardware, including flexibility, modularity, scalability and reusability. Then, we demonstrate the main features of the open-source ESP infrastructure, including integration of third-party RISC-V cores and accelerators developed with various design flows (high-level synthesis, Chisel, RTL), system-level ESP services for managing heterogeneity, and reconfigurable cache-coherence models for accelerators. Finally, we illustrate the ESP software-stack templates that enable system-level simulation for testing accelerators with bare-metal applications and full-system FPGA-based emulation for software development.

BIOGRAPHIE(S):

Luca P. Carloni is Professor of Computer Science at Columbia Univ. in the City of New York. He holds a Laurea Degree in Electronics Engineering from the Univ. of Bologna and the MS and PhD degrees in Electrical Engineering and Computer Sciences from UC Berkeley. His research interests are in system-on-chip platforms and distributed embedded systems. He coauthored over one hundred and forty refereed papers. Luca received the NSF CAREER Award, the ONR Young Investigator Award, and an Alfred P. Sloan Research Fellowship. In 2013, Luca served as general chair of Embedded Systems Week. Luca is an IEEE Fellow.

Giuseppe Di Guglielmo received the Laurea degree (summa cum laude) and the PhD degree in Computer Science from the Univ. of Verona, Italy in 2005 and 2009, respectively. He is currently an Associate Research Scientist with the Department of Computer Science, Columbia Univ., New York. His PhD thesis was on the verification and validation of system-level hardware design. His current research topics include the design, validation, and security of hardware accelerators. He is also interested in the acceleration of machine learning applications for physics and robotics with high-level synthesis and FPGA platforms. He has authored over 50 publications.

Davide Giri is a PhD student in Computer Science at Columbia Univ.. He received the MS degree in electronic engineering from Politecnico di Torino and the MS degree in electrical and computer engineering from the Univ. of Illinois at Chicago. His research interests include architectures and system-level design methodologies for heterogeneous system-on-chip. Contact him at davide.giri@columbia.edu.

Paolo Mantovani is an Associate Research Scientist at Columbia Univ.. He earned the MS in Electronic Engineering at Politecnico di Torino and the PhD in Computer Science at Columbia Univ.. His PhD and current research interests include architecture design and system-level methodologies for the integration and programming of heterogeneous computing platforms. Paolo contributes to the open-source hardware community as the main architect of the `Embedded Scalable Platforms` architecture and FPGA emulation infrastructure.

Tutorial 3 - Machine Learning for Design and Optimization of Embedded Systems

Time: 9:00 - 13:00 | Room: Furman Hall 214

Organizer:

Jana Doppa - *Washington State Univ.*

Speakers:

Jana Doppa - *Washington State Univ.*
Philip Brisk - *Univ. of California, Riverside*

The rate of growth of Big Data, slowing down of Moore's law, and the rise of emerging applications pose significant challenges in the design of large-scale computing systems with high-performance, energy-efficiency, and reliability. This tutorial will consider solutions based on machine learning and data analytics to address these challenges. Some specific topics include:

1. How to use machine learning and statistical modeling for effective design space exploration of computing systems to optimize for power, performance, and thermal metrics?

2. How to use machine learning techniques to efficiently manage resources of computing systems (e.g., power, memory, interconnects) to improve performance and energy-efficiency?

3. How to use machine learning techniques same-generation GPU prediction, cross-generation GPU prediction, and CPU to FPGA prediction?

BIOGRAPHIE(S):

Jana Doppa is the George and Joan Berry Assistant Professor in the School of EECS at Washington State Univ., Pullman. He earned his PhD working with the AI group at Oregon State Univ. (2014); and his M.Tech from Indian Institute of Technology, Kanpur, India (2006). His current research interests are at the intersection of machine learning and electronic design automation. He received NSF CAREER Award (2019), an Outstanding Paper Award at the AAAI (2013) conference, a Google Faculty Research Award (2015), the Outstanding Innovation in Technology Award from OSU (2015), and a Outstanding Reviewer Award at the NeurIPS (2018) conference.

Philip Brisk received the B.S., M.S., and Ph.D., all in Computer Science, from UCLA in 2002, 2003, and 2006 respectively. From 2006-2009, he was a postdoctoral scholar at EPFL in Lausanne, Switzerland. Since 2009, he has been with the Univ. of California, Riverside; he has been promoted to Professor effective July 1, 2019. Dr. Brisk's research interests lie at the intersection between processor architecture, VLSI/CAD, compilers, FPGAs, and reconfigurable computing; most recently, he has been applying these principles to the design and analysis of biological instruments. He is a Senior Member of the ACM and IEEE, and is presently an Associate Editor of the IEEE Transactions of Computer-Aided Design on Integrated Circuits and Systems (TCAD) and Integration: The VLSI Journal.

Tutorial 4 - HW/SW Modeling and Performance Analysis of Heterogeneous Safety-Critical Systems

Time: 14:00 - 18:00 | Room: Furman Hall 210

Organizers:

Selma Saidi - *Hamburg Univ. of Technology*
Arne Hamann - *Robert Bosch GmbH*

Speakers:

Dirk Ziegenbein - *Robert Bosch GmbH*
Helmar Wieland - *INCHRON GmbH*
Rafik Henia - *Thales Research and Technology*
Selma Saidi - *Hamburg Univ. of Technology*

The current trend in safety-critical systems towards automation and connectivity imposes an increased complexity and hardware/software system heterogeneity. This trend tremendously challenges established modeling and performance analysis methods and tools used for the design of safe and correct systems where particularly stringent requirements on worst-case response times and end-to-end latencies need to be met.

The tutorial will highlight recent challenges in modeling and timing analysis of safety-critical systems recently integrated on general-purpose heterogeneous MPSoCs platforms. The tutorial will cover performance analysis considering formal timing analysis approaches dedicated to shared network and memory resources as well as simulation for the analysis of dynamic behavior of software. The tutorial will also present Time4Sys, an open source pivot model that addresses the fundamental issue of the semantic gap between the various design languages and their underlying timing concepts present in existing timing analysis frameworks. The tutorial will besides introduce AMALTHEA, an open source data format for performance modeling, simulation, and analysis of embedded and automotive systems.

BIOGRAPHIE(S):

Dirk Ziegenbein is chief expert for engineering of cyber-physical systems at Robert Bosch Corporate Research. Additionally, he leads a team of 20 experts researching software systems engineering methods for cyber-physical systems in automotive, robotics and IoT. Dirk received a Ph.D. degree from Technical Univ. of Braunschweig for his dissertation on modeling and design automation of embedded systems. In 2002, Dirk joined Bosch Research and worked on topics such as software component technology and scheduling analysis. From 2007 to 2012, he was responsible for the product management of embedded software engineering tools at ETAS GmbH.

Helmar Wieland graduated in 2007 from Friedrich-Alexander-Univ. of Erlangen-Nuremberg with a degree in computer science. For his diploma thesis, he created a timing accurate simulator for cache memories for his future employer, INCHRON GmbH. Since then, he has stayed true to the real-time community. In various positions, he is driving the advancement of chronSIM, the real-time simulator and INCHRON's core product, training its users and helping them design excellent and robust system and software architectures. He also has more than 10 years of experience conducting customer projects with the automotive industry's leading OEMs and Tier-1s.

Rafik Henia graduated from the Technical Univ. of Braunschweig in 2003 where he worked as a researcher at the Institute of Computer and Network Engineering with research topics related to the timing verification for real-time embedded systems. Since 2009, he has been a research engineer at Thales Research and Technology France, in the Critical Embedded Systems Lab. He works in collaboration with Thales avionics, aerospace, telecommunication and defense divisions on R&D projects mostly focusing on the integration of model-based performance design and verification techniques in the industrial development process of real-time embedded systems.

Arne Hamann obtained his PhD in Computer Science in 2008 from the Technical Univ. of Braunschweig, Germany. His PhD thesis was awarded the EDAA Outstanding Dissertation Award 2009 in the category "New directions in embedded system design and embedded software". Currently, Arne Hamann is working for Bosch Corporate Research in the division of "Software-intensive Systems". There, he acts as a chief expert for distributed intelligent systems and real-time system design principles for physically dominated embedded systems. Additionally, he regularly serves as program committee members for international conferences such as ECRTS, DAC, EMSOFT, RTSS, DSD, and ETFA.

Selma Saidi received a Ph.D from the Univ. of Grenoble in 2012 working jointly with STMicroelectronics on optimizing memory transfers for a new generation of embedded multicore architectures. Later she joined the Technical Univ. of Braunschweig as a post doctoral researcher to work on embedded multi-core platforms dedicated to real-time and safety critical systems. Currently, she has a permanent research position in Hamburg Univ. of Technology. Her research interests involve developing new timing analysis methods for hardware components in MPSoCs, in addition to novel HW/SW mechanisms to ensure efficient and safe sharing of resources in heterogeneous systems.

Tutorial 5 - Machine Learning Security

Time: 9:00 - 13:00 | Room: Furman Hall 210

Organizer:

Siddharth Garg - *New York Univ.*

Speakers:

Muhammad Shafique - *Vienna Univ. of Technology*
Siddharth Garg - *New York Univ*
Brendan Dolan-Gavitt - *New York Univ*

With the growing use of artificial intelligence (AI) and machine learning (ML) techniques in a wide range of domains, questions about their safety, security and privacy are of growing importance. A growing body of work suggests that modern AI and ML techniques are vulnerable to attack. Attacks include stealthy training data poisoning attacks, and so-called ``adversarial input perturbations" which have to been shown to be particularly pernicious for deep neural networks. Further, as deep learning systems are often trained and executed in the cloud, concerns about the privacy of the user's data and the IP rights of the model's owner must be addressed. This tutorial will provide a comprehensive overview of a range of integrity and privacy attacks and emerging defense mechanisms.

BIOGRAPHIE(S):

Siddharth Garg received his Ph.D. degree in ECE from Carnegie Mellon Univ. in 2009, and a B.Tech. degree in EE from the Indian Institute of Technology Madras. He joined NYU in Fall 2014 as an Assistant Professor. His general research interests are in computer engineering, and more particularly in secure, reliable and energy-efficient computing. In 2016, Siddharth was listed in Popular Science Magazine's annual list of "Brilliant 10" researchers. Siddharth has received the NSF CAREER Award (2015), and paper awards at IEEE Symposium on Security and Privacy (S&P) 2016 and USENIX Security Symposium 2013.

Muhammad Shafique is a full professor (Univ. Prof.) of Computer Architecture and Robust Energy-Efficient Technologies (CARE-Tech.) at the Embedded Computing Systems Group, Institute of Computer Engineering, Faculty of Informatics, Vienna Univ. of Technology (TU Wien) since Nov. 2016. He received his Ph.D. in Computer Science from Karlsruhe Institute of Technology (KIT), Germany in Jan.2011. His research interests are in energy-efficient, dependable & fault-tolerant system design, hardware security, machine Learning and AI, and embedded systems. Dr. Shafique received 2015 ACM/SIGDA Outstanding New Faculty Award and several best paper awards and nominations at prestigious conferences like CODES+ISSS, DATE, DAC and ICCAD.

Brendan Dolan-Gavitt is currently an Assistant Professor in the Computer Science and Engineering Department at the NYU Tandon School of Engineering. His research interests include program analysis, virtualization security, machine learning security and embedded and cyber-physical systems. Currently, his research focuses on developing techniques to ease or automate the understanding of large, real-world software systems in order to develop novel defenses against attacks. He received his PhD from Georgia Tech in August 2014, and a B.A. in Mathematics and Computer Science from Wesleyan Univ. in 2006.

Tutorial 6 - Industry Tutorial: PYNQ: Python Productivity for Zynq

Time: 14:00 - 18:00 | Room: Furman Hall 212

Organizer:

Parimal Patel - *Xilinx Univ. Program (XUP)*

Speakers:

Parimal Patel - *Xilinx Univ. Program*

PYNQ is an open-source framework (http://www.pynq.io/) that enables programmers who want to use embedded systems to exploit the capabilities of Xilinx Zynq SoCs, which are processor-centric platforms that offer software-, hardware- and I/O-level programmability in a single chip. It allows users to exploit custom hardware in the programmable logic without having to use ASIC-style CAD tools. Instead the SoC is programmed in Python and the code is developed and tested directly on the embedded system. The programmable logic circuits are imported as hardware libraries and programmed through their APIs, in essentially the same way that software libraries are imported and programmed.

The framework combines four main elements: (1) the use of a high-level productivity language, Python in this case; (2) Python-callable hardware libraries based on FPGA overlays; (3) a web-based architecture incorporating the open-source Jupyter Notebook infrastructure served from Zynq's embedded processors; and (4) Jupyter Notebook's client-side, web apps. The result is a web-centric programming environment that enables software programmers to work at higher levels of design abstraction and to re-use both software and hardware libraries.

This tutorial will give a hands-on introduction to PYNQ framework using PYNQ-Z2 board. It will feature the latest PYNQ release which includes an updated API, an optimized video pipeline, a simplified way of integrating new hardware and drivers into PYNQ, partial reconfiguration support, and developing, compiling, and deploying C-language code straight from the Jupyter notebook without opening Xilinx SDK tool. The tutorial will also include demonstration of some notebook examples of how the framework can be used in in the development, testing and modeling of cyber-physical systems.

BIOGRAPHIE(S):

Parimal Patel received a Doctor of Philosophy in Electrical and Computer Engineering from the Univ. of Texas at Austin, Texas in 1986.

In 1987 he joined the Univ. of Texas as an Assistant Professor, got promoted to Associate and then to Full Professorships. During his tenure at the Univ. he taught variety of courses including Logic Design, Digital Systems Design, Microcomputer Systems (peripheral interface principles), Embedded Systems Design, VLSI System Design, Computer Architecture, RISC Processor Design, Engineering Workstations, and Advanced HDL modeling.

Parimal has always enjoyed teaching and developing new courses. He started as a contract trainer and then full-time employee of Xilinx developing variety of courses for Customer Education department. He joined the Xilinx Univ. Program in April 2007 developing new courses, updating current courses, and delivering XUP workshops worldwide, including High-Level Synthesis, Embedded Systems, Advanced Embedded Systems, DSP Design Flow, DSP Implementation Techniques, Designing with SDSoC, Dynamic Partial Reconfiguration, Python Productivity on Zynq (PYNQ), and Accelerated Cloud Computing on AWS with SDAccel.

Tutorial 7 - Industry Tutorial: The Open Source ACRN Hypervisor on an Intel Embedded Platform

Time: 9:00 - 13:00 | Room: Furman Hall 212

Organizer:

Kashif Rajput - *Intel Corp.*

Speakers:

Kashif Rajput - *Intel Corp.*
Sainath Grandhi - *Intel Corp.*

Project ACRN pronounced (ACORN), was launched as a Linux Foundation project on March'18. This is an open source lightweight device hypervisor, specifically designed for Internet of Things (IoT) workload consolidation use cases. In addition to be small footprint, Project ACRN is designed with Function Safety & real time in mind, which are two highly critical requirements in IoT.

This tutorial will explain/show case at length Intel's Hypervisor initiative known as ACRN and also teach how to get access to its open source code, compile/build and then load it on an Intel Embedded platform for various emerging Industry virtualization use cases. A virtualized environment will be setup on Intel's Apollo Lake embedded hardware reference platform and then Android Guest OS will be configured to run on it. Once done with the virtualized environment setups, the various aspects of selecting system parameters to measure and configure performance will be discussed along with the tools involved. Finally the tutorial will cover the IoT use cases of ACRN hypervisor in the Automotive segment and Industrial Segment.

Pre-requisites:

* Familiarity with Linux OS and Android OS

* Familiarity with BSP Development Concepts

* Comfortable with handling Hardware Reference boards/dev kits

* Familiarity with Virtualization concepts

BIOGRAPHIE(S):

Kashif Rajput is a Software Architect with Intel's Internet of Things Group (IOTG), leading the Android BSP (Board Support Package) Software Development within IOTG. Industry software development experience of around 20 years with focused 13 years' experience in Embedded BSP development on various operating systems such as VxWorks, Embedded Linux, WinCE and now Android. Kashif holds a Master's degree in Software Engineering.

Sainath Grandhi is a Software Engineer with Virtualization Group in Intel. Experience working with hypervisors, KVM and ACRN. Prior to working in Virtualization group, experience in power management and scheduler optimizations for Windows Kernel. Sainath holds Master's degree in Computer Engineering.

MONDAY, OCTOBER 14
SCHEDULE OF EVENTS

	KC 405/406	KC 914	KC 905/907
08:15 - 09:00	**ESWEEK Opening Session** | Room: Eisner Lubin Auditorium		
09:00 - 10:00	**KEYNOTE**: *"High Performance Computing in a World of Embedded Intelligence", Steve Keckler, NVIDIA* | Room: Eisner Lubin Auditorium		
10:00 - 10:30	Coffee Break | Room: Eisner Lubin Auditorium		
10:30 - 12:00	**CASES:** *Neural Networks Optimization*	**CODES+ISSS:** *Embedded and IoT Applications*	**EMSOFT:** *Modeling and Design I*
12:00 - 12:30	**Poster Session** | Room: Eisner Lubin Auditorium		
12:30 - 13:30	Lunch | Room: Eisner Lubin Auditorium		
13:30 - 15:00	**CASES:** *Accelerator Design*	**CODES+ISSS:** *Memory and Storage Systems*	**EMSOFT:** *Verification and Runtime Monitoring*
15:00 - 15:30	**Poster Session & Coffee Break** | Room: Eisner Lubin Auditorium		
15:30 - 17:00	**Special Session:** *The Information Processing Factory - a Paradigm for Long-term Dependable Systems*	**CODES+ISSS:** *Embedded Machine Learning*	**EMSOFT:** *Timing, Scheduling and Parallel Execution*
17:00 - 17:30	**Poster Session** | Room: Eisner Lubin Auditorium		

Opening Session

Time: 8:15 - 9:00 | Room: Eisner Lubin Auditorium

Keynote: High Performance Computing in a World of Embedded Intelligence

Time: 9:00 - 10:00 | Room: Eisner Lubin Auditorium

Speaker:
Steve Keckler - *NVIDIA, Corp.*

The confluence of high-performance computing and massive training data sets has enabled machine learning algorithms to play a transformational role in many disciplines. While tremendous effort has been applied to both training and inference in datacenter settings, the world of embedded computing devices demands capabilities to perceive entities in a complex environment, understand their surroundings, and make intelligent decisions based on observations. Applications such as intelligent video analytics, autonomous vehicles, and robotics all have tremendous computational requirements, limited power budgets, and safety/privacy standards that must be met. This talk will describe requirements of these embedded intelligence workloads and opportunities for architecture and hardware/software co-design to provide the computational throughput within the requisite power envelopes. It will also discuss challenges for safety-critical systems and methods of understanding and mitigating such vulnerabilities. Finally, the talk will present an automated design methodology for customizing an architecture to the specific parameters of a machine learning application, enabling quick development of optimized ASIC designs.

Biography: Dr. Stephen W. Keckler is the Vice President of Architecture Research at NVIDIA and an Adjunct Professor of Computer Science at the University of Texas at Austin, where he served on the faculty from 1998-2012. His research interests include parallel computer architectures, high-performance computing, energy-efficient architectures, and embedded computing. Dr. Keckler is a Fellow of the ACM, a Fellow of the IEEE, an Alfred P. Sloan Research Fellow, and a recipient of the NSF CAREER award, the ACM Grace Murray Hopper award, the President's Associates Teaching Excellence Award at UT-Austin, and the Edith and Peter O'Donnell award for Engineering. He earned a B.S. in Electrical Engineering from Stanford University and M.S. and Ph.D. degrees in Computer Science from the Massachusetts Institute of Technology

Session 1A - CASES: Neural Networks Optimization

Time: 10:30 - 12:00 | Room: KC 405/406

Chair:

Umit Ogras - *Arizona State Univ.*

1A.1 TF-NET: DEPLOYING SUB-BYTE DEEP NEURAL NETWORKS ON MICROCONTROLLERS

Jiecao Yu - *Univ. of Michigan*
Andrew Lukefahr - *Indiana Univ.*
Reetuparna Das, Scott Mahlke - *Univ. of Michigan*

1A.2* AGGRESSIVE ENERGY REDUCTION FOR VIDEO INFERENCE WITH SOFTWARE-ONLY STRATEGIES

Larissa Rozales Gonçalves - *Univ. Federal do Rio Grande do Sul*
Rafael Fão de Moura - *Univ. Federal do Rio Grande do Sul*
Luigi Carro - *Univ. Federal do Rio Grande do Sul*

1A.3 COMPACT: ON-CHIP COMPRESSION OF ACTIVATIONS FOR LOW POWERSYSTOLIC ARRAY BASED CNN ACCELERATION

Jeff Zhang, Parul Raj - *New York Univ.*
Shuayb Zarar, Amol Ambardekar - *Microsoft*
Siddharth Garg - *New York Univ.*

Session 1B - CODES+ISSS: Embedded and IoT Applications

Time: 10:30 - 12:00 | Room: KC 914

Chair:

Amlan Ganguly - *Rochester Institute of Technology*

Co-Chair:

Tosiron Adegbija - *Univ. of Arizona*

1B.1 SWARAM: PORTABLE ENERGY AND COST EFFICIENT EMBEDDED SYSTEM FOR GENOMIC PROCESSING

Ram Mohanty, Hasindu Gamaarachchi, Andrew Lambert, Sri Parameswaran - *Univ. of New South Wales*

1B.2 AUTHCROPPER: AUTHENTICATED IMAGE CROPPER FOR PRIVACY PRESERVING SURVEILLANCE SYSTEMS

Jihye Kim - *Kookmin Univ.*
Jiwon Lee, **Hankyung Ko**, Donghwan Oh, Semin Han, Gwonho Jeong, Hyunok Oh - *Hanyang Univ.*

1B.3 OPTODE DESIGN SPACE EXPLORATION FOR CLINICALLY-ROBUST NON-INVASIVE FETAL OXIMETRY

Daniel D. Fong, Vivek J. Srinivasan, Kourosh Vali, Soheil Ghiasi - *Univ. of California, Davis*

Session 1C - EMSOFT: Modeling and Design I

Time: 10:30 - 12:00 | Room: KC 905/907

Chair:

Edward A. Lee - *Univ. of California, Berkeley*

1C.1* DERIVING EQUATIONS FROM SENSOR DATA USING DIMENSIONAL FUNCTION SYNTHESIS

Sam Willis, Youchao Wang, **Vasileios Tsoutsouras** - *Cambridge Univ.*
Phillip Stanley-Marbell - *Massachusetts Institute of Technology*

1C.2 A DUAL-MODE STRATEGY FOR PERFORMANCE-MAXIMISATION AND RESOURCE-EFFICIENT CPS DESIGN

Xiaotian Dai, **Wanli Chang**, Shuai Zhao, Alan Burns - *Univ. of York*

1C.3 COHERENT EXTENSION, COMPOSITION, AND MERGING OPERATORS IN CONTRACT MODELS FOR SYSTEM DESIGN

Roberto Passerone - *Univ. of Trento*
Íñigo Íncer-Romeo, Alberto Sangiovanni Vincentelli - *Univ. of California, Berkeley*

** Denotes Best Paper Candidate*

Poster Session

Time: 12:00 - 12:30 | Room: Eisner Lubin Auditorium

Session 2A - CASES: Accelerator Design

Time: 13:30 - 15:00 | Room: KC 405/406

Chair:
Henri-Pierre Charles - *CEA*

2A.1 ECAX: BALANCING ERROR CORRECTION COSTS IN APPROXIMATE ACCELERATORS
Jorge Castro-Godínez - *Karlsruhe Institute of Technology*
Muhammad Shafique - *Vienna Univ. of Technology*
Joerg Henkel - *Karlsruhe Institute of Technology*

2A.2* AN ULTRA-LOW ENERGY HUMAN ACTIVITY RECOGNITION ACCELERATOR FOR WEARABLE HEALTH APPLICATIONS
Ganapati Bhat, Yigit Tuncel, Sizhe An - *Arizona State Univ.*
Hyung Gyu Lee - *Daegu Univ.*
Umit Ogras - *Arizona State Univ.*

2A.3 WORK-IN-PROGRESS: COMPUTATION OFFLOADING OF ACOUSTIC MODEL FOR CLIENT-EDGE-BASED SPEECH RECOGNITION
Young Min Lee, Joon-Sung Yang - *Sungkyunkwan Univ.*

2A.4 WORK-IN-PROGRESS: FINE-GRAIN ACCELERATION USING RUNTIME INTEGRATED CUSTOM EXECUTION (RICE)
Leela Pakanati, John T. McMichen, Zachary Estrada - *Rose-Hulman Institute of Technology*

2A.5 WORK-IN-PROGRESS: ECC MANAGEMENT WITH RATE COMPATIBLE LDPC CODE FOR NAND FLASH STORAGE
Seung-Ho Lim, Jae-Bin Lee, Geon-Myeong Kim - *Hankuk Univ. of Foreign Studies*

2A.6 WORK-IN-PROGRESS: AUTOMATIC GENERATION OF APPLICATION-SPECIFIC FPGA OVERLAYS
Danielle Tchuinkou Kwadjo, **Joel Mandebi Mbongue**, Christophe Bobda - *Univ. of Florida*

2A.7 WORK-IN-PROGRESS: RECONFIGURABLE ACCELERATOR ON FPGA FOR SCIENTIFIC COMPUTING
Juan Pedro Cobos Carrascosa, D. Hernández Expósito, J.L. Ramos Mas, B. Aparicio del Moral, A. Sánchez Gómez, M. Balaguer, A.C. López Jiménez, Orozco Suárez, J.C. del Toro Iniesta - *Instituto de Astrofísica de Andalucía*

* *Indicates Best Paper Candidate*

Session 2B - CODES+ISSS: Memory and Storage Systems

Time: 13:30 - 15:00 | Room: KC 914

Chair:
Jingtong Hu - *Univ. of Pittsburgh*

Co-Chair:
Andreas Gerstlauer - *Univ. of Texas, Austin*

2B.1 PREDICTNCOOL: LEAKAGE AWARE THERMAL MANAGEMENT FOR 3D MEMORIES USING A LIGHTWEIGHT TEMPERATURE PREDICTOR
Lokesh Siddhu - *Indian Institute of Technology, Delhi*
Preeti Ranjan Panda - *Indian Institute of Technology Delhi*

2B.2 RMW-F: A DESIGN OF RMW-FREE CACHE USING BUILT-IN NAND-FLASH FOR SMR STORAGE
Chenlin Ma - *Hong Kong Polytechnic Univ.*
Zhaoyan Shen - *Shandong Univ.*
Lei Han - *Hong Kong Polytechnic Univ.*
Zili Shao - *Chinese Univ. of Hong Kong*

2B.3 ENABLING SEQUENTIAL-WRITE-CONSTRAINED B+-TREE INDEX SCHEME TO UPGRADE SHINGLED MAGNETIC RECORDING STORAGE PERFORMANCE
Yu-Pei Liang - *National Tsing Hua Univ.*
Tseng-Yi Chen - *Yuan Ze Univ.*
Yuan-Hao Chang, Shuo-Han Chen - *Academia Sinica*
Kam-Yiu Lam - *City Univ. of Hong Kong*
Wei-Hsin Li, Wei-Kuan Shih - *National Tsing Hua Univ.*

Session 2C - EMSOFT: Verification and Runtime Monitoring

Time: 13:30 - 15:00 | Room: KC 905/907

Chair:
Borzoo Bonakdarpour - *Iowa State Univ.*

2C.1 EFFICIENT DECENTRALIZED LTL MONITORING FRAMEWORK USING TABLEAU TECHNIQUE
Omar Bataineh - *Nanyang Technological Univ.*
David Rosenblum - *National Univ. of Singapore*
Mark Reynolds - *Univ. of West Alabama*

2C.2 FPGA STREAM-MONITORING OF REAL-TIME PROPERTIES
Jan Baumeister, Bernd Finkbeiner, **Maximilian Schwenger**, Hazem Torfah - *Saarland Univ.*

2C.3 WILL MY PROGRAM BREAK ON THIS FAULTY PROCESSOR? - FORMAL ANALYSIS OF HARDWARE FAULT ACTIVATIONS IN CONCURRENT EMBEDDED SOFTWARE
Levente Bajczi - *Budapest Univ. of Technology and Economics*
András Vörös - *Massachusetts Institute of Technology*
Vince Molnár - *Budapest Univ. of Technology and Economics*

** Indicates Best Paper Candidate*

Poster Session & Coffee Break

Time: 15:00 - 15:30 | Room: Eisner Lubin Auditorium

Special Session 3A: The Information Processing Factory - A Paradigm for Life Cycle Management of Dependable Systems

Time: 15:30 - 17:00 | Room: KC 405/406

Chair:

Sankar Basu - *National Science Foundation (NSF)*

Organizers:

Rolf Ernst - *Technische Univ. Braunschweig*
Nikil Dutt - *Univ. of California, Irvine*
Fadi Kurdahi - *Univ. of California, Irvine*
Andreas Herkersdorf - *Technische Univ. München*

The number and complexity of embedded system platforms used in mixed-criticality applications are rapidly growing. They run large and evolving applications on heterogeneous multi-/many-core processing platforms requiring long term dependable operation. Examples include automated driving, smart buildings, industry 4.0, or personal medical devices. A 2016 ESWEEK special session gave an overview of state of the art in self-aware HW/SW system technology which could become an important basis for mastering complex dependable systems. The session presentations explained types and implementations of self-awareness and compared different approaches, including on-the-fly computing, self-aware platform control, and cross-layer self-awareness. One of the talks introduced the paradigm of an "Information Processing Factory" (IPF). An abstract concept at that time, IPF has been further elaborated and became the foundation of a US-German research initiative for research into detailed solutions and applications. IPF applies principles inspired by factory management to the continuous operation and optimization of highly-integrated embedded systems. A general objective is identifying a sweet spot between a maximum of autonomy among IPF constituent components and a minimum of centralized control in order to ensure guaranteed service even under strict safety and availability requirements. Emphasis is on intensive self- diagnosis for early detection of degradation and imminent failures combined with unsupervised platform self-adaptation to meet performance and safety targets. The initiative developed into a research cluster that is jointly funded by the NSF and DFG. The cluster exploits a variety of technologies including proactive reconfiguration to mitigate the risk of failures, self-optimization, and self-identification using learning classifiers, and chip-level operation with flexible boundaries between critical and best effort regions, all guided by a self-aware planning component. A large many-core multi-OS simulation platform provides the means for in-depth cross-layer experiments.

3A.1 INTRODUCTION TO THE IPF PLATFORM AND RESEARCH CLUSTER

Rolf Ernst - *Technische Univ. Braunschweig*

3A.2 PROACTIVE SELF-DIAGNOSIS AND TASK MIGRATION FOR SAFETY-CRITICAL APPLICATIONS

Eberle A. Rambo, Thawra Kadeed, **Rolf Ernst** - *Technische Univ. Braunschweig*

3A.3 IPF RUNTIME VERIFICATION

Minjun Seo, **Fadi Kurdahi** - *Univ. of California, Irvine*

3A.4 REFLECTIVE SUPERVISORY CONTROL IN HIERARCHICAL MACHINE LEARNING

Bryan Donyanavard, Caio Batista de Melo, Biswadip Maity, Kasra Moazzemi, Kenneth Stewart, Saehanseul Yi, Amir M. Rahmani, **Nikil Dutt** - *Univ. of California, Irvine*

3A.5 HARDWARE-BASED LEARNING CLASSIFIERS FOR MIXED-CRITICAL ENVIRONMENTS

Nguyen Anh Vu Doan, Florian Maurer, Anmol Surhonne, Thomas Wild, **Andreas Herkersdorf** - *Technische Univ. München*

** Indicates Best Paper Candidate*

Session 3B - CODES+ISSS: Embedded Machine Learning

Time: 15:30 - 17:00 | Room: KC 914

Chair:

Janardhan Doppa - *Washington State Univ.*

3B.1* ACHIEVING SUPER-LINEAR SPEEDUP ACROSS MULTI-FPGA FOR REAL-TIME DNN INFERENCE

Weiwen Jiang - *Univ. of Pittsburgh*
Edwin Sha - *East China Normal Univ.*
Xinyi Zhang - *Univ. of Pittsburgh*
Lei Yang - *Chongqing Univ.*
Qingfeng Zhuge - *East China Normal Univ.*
Yiyu Shi - *Univ. of Notre Dame*
Jingtong Hu - *Univ. of Pittsburgh*

3B.2* ACHIEVING LOSSLESS ACCURACY WITH LOSSY PROGRAMMING FOR EFFICIENT NEURAL-NETWORK TRAINING ON NVM-BASED SYSTEMS

Wei-Chen Wang - *Macronix International Co., Ltd.*
Yuan-Hao Chang - *Academia Sinica*
Tei-Wei Kuo - *National Taiwan Univ.*
Chien-Chung Ho - *National Chung Cheng Univ.*
Yu-Ming Chang - *National Taiwan Univ.*
Hung-Sheng Chang - *Macronix International Co., Ltd.*

3B.3 DWMACC: ACCELERATING SHIFT-BASED CNNS WITH DOMAIN WALL MEMORIES

Zhengguo Chen, Quan Deng - *National Univ. of Defense Technology*
Nong Xiao - *Sun Yat-sen Univ.*
Kirk Pruhs, Youtao Zhang - *Univ. of Pittsburgh*

** Indicates Best Paper Candidate*

Session 3C - EMSOFT: Timing, Scheduling and Parallel Execution

Time: 15:30 - 17:00 | Room: KC 905/907

Chair:
Houssam Abbas - *Oregan State Univ.*

3C.1 THERMAL-AWARE SCHEDULING FOR INTEGRATED CPUS-GPU PLATFORMS
Youngmoon Lee - *Univ. of Michigan*
Hoonsung Chwa - *Daegu Gyeongbuk Institute of Science and Technology*
Kang G. Shin - *Univ. of Michigan*

3C.2 TIMING-ANOMALY FREE DYNAMIC SCHEDULING OF CONDITIONAL DAG TASKS ON MULTI-CORE SYSTEMS
Peng Chen, Xu Jiang, Qingqiang He - *Hong Kong Polytechnic Univ.*
Weichen Liu - *Nanyang Technological Univ.*
Nan Guan - *Hong Kong Polytechnic Univ.*

3C.3 WORK-IN-PROGRESS: PROGRAMS WITH IRONCLAD TIMING GUARANTEES
Marten Lohstroh - *Univ. of California, Berkeley*
Martin Schoeberl - *Technical Univ. of Denmark*
Mathieu Jan - *CEA*
Edward Wang, Edward A. Lee - *Univ. of California, Berkeley*

3C.4 WORK-IN-PROGRESS: AN ILP FRAMEWORK FOR ENERGY OPTIMIZED SCHEDULING FOR WEAKLY-HARD REAL-TIME SYSTEMS
Jaishree Mayank, **Niraj Kumar**, Arijit Mondal - *Indian Institute of Technology Patna*

3C.5 WORK-IN-PROGRESS: WHY STATISTICAL POWER MATTERS FOR PROBABILISTIC REAL-TIME
Federico Reghenzani - *Politecnico di Milano*
Luca Santinelli - *ONERA*
William Fornaciari - *Politecnico di Milano*

3C.6 WORK-IN-PROGRESS: DAPHNE - AN AUTOMOTIVE BENCHMARK SUITE FOR PARALLEL PROGRAMMING MODELS ON EMBEDDED HETEROGENEOUS PLATFORMS
Lukas Sommer, Leonardo Solis-Vasquez, Florian Stock, Andreas Koch - *Technische Univ. Darmstadt*

Poster Session

Time: 17:00 - 17:30 | Room: Eisner Lubin Auditorium

* Denotes Best Paper Candidate

TUESDAY, OCTOBER 15
SCHEDULE OF EVENTS

	KC405	KC802	KC905/907	KC406
09:00 - 10:00	**KEYNOTE**: "Health Monitoring with Machine Learning and Wireless Sensors", Dina Katabi, MIT | Room: Eisner Lubin Auditorium			
10:00 - 10:30	Coffee Break | Room: Eisner Lubin Auditorium			
10:30 - 12:00	**CASES:** *Interconnect Design*	**CODES+ISSS:** *Domain Specific Optimizations*	**EMSOFT:** *Verification and Testing*	**Special Session IoMT:** *Cyber-Physical Monitoring, Diagnosis, Treatment Analysis and Online Therapy*
12:00 - 12:30	**Poster Session** | Room: Eisner Lubin Auditorium			
12:30 - 13:30	Lunch | Room: Eisner Lubin Auditorium			
13:30 - 15:00	**CASES:** *Emerging Technologies*	**CODES+ISSS:** *Adaptive and Intermittent Embedded Systems*	**EMSOFT:** *Modeling and Design II*	**Special Session IoMT:** *Deciphering the Brain: From Mathematical Models to Computing Platforms for Cyber-Human Autonomy Symbiosis*
15:00 - 15:15	Break | Room: Eisner Lubin Auditorium (Posters related to the papers presented Tuesday after lunch will be on display in the poster session on Wednesday 10:00 - 10:30)			
15:15 - 16:45	**CASES:** *Embedded Systems Design*	**CODES+ISSS:** *Reliability, Security, and Timing*	**EMSOFT:** *Hybrid Systems*	**Special Session IoMT:** *Security, Privacy, Dependability, Reliability and Resieliency in IoMT*
17:30 - 22:00	**Social Event - Carmine's Restaurant in Times Sq & Broadway Show**			

Keynote: Health Monitoring with Machine Learning and Wireless Sensors

Time: 9:00 - 10:00 | Room: Eisner Lubin Auditorium

Speaker:
Dina Katabi - *MIT*

This talk will introduce Emerald, a new wireless technology that uses machine learning for health monitoring in the home. The Emerald device is a Wi-Fi like box that transmits low power radio signals, and analyzes their reflections using neural networks. It infers the movements, breathing, heart rate, falls, sleep apnea, and sleep stages, of people in the home -- all without requiring them to wear any sensors or wearables. By monitoring a variety of physiological signals continuously and without imposing a burden on users, Emerald can automatically detect degradation in health, enabling early intervention and care. The talk will describe the underlying technology, and present results demonstrating Emerald's promise in a geriatric population.

Biography: Dina Katabi is the Andrew & Erna Viterbi Professor of Electrical Engineering and Computer Science at MIT. She is also the director of the MIT's Center for Wireless Networks and Mobile Computing, a member of the National Academy of Engineering, and a recipient of the MacArthur Genius Award. Professor Katabi received her PhD and MS from MIT in 2003 and 1999, and her Bachelor of Science from Damascus University in 1995. Katabi's research focuses on innovative mobile and wireless technologies with particular application to digital health. Her research has been recognized by the ACM Grace Murray Hopper Award, the SIGCOMM test of Time Award, the Faculty Research Innovation Fellowship, a Sloan Fellowship, the NBX Career Development chair, and the NSF CAREER award. Her students received the ACM Best Doctoral Dissertation Award in Computer Science and Engineering twice. Further, her work was recognized by the IEEE William R. Bennett prize, three ACM SIGCOMM Best Paper awards, an NSDI Best Paper award, and a TR10 award. Several start-ups have been spun out of Katabi's lab such as PiCharging and Emerald..

Session 4A - CASES: Interconnect Design

Time: 10:30 - 12:00 | Room: KC 405

Chair:

Pietro Mercati - *Intel Corp.*

4A.1 CASCADE: HIGH THROUGHPUT DATA STREAMING VIA DECOUPLED ACCESS/EXECUTE CGRA

Dhananjaya Wijerathne, Zhaoying Li, Manupa Karunaratne, Anuj Pathania, Tulika Mitra - *National Univ. of Singapore*

4A.2 IS YOUR BUS ARBITER REALLY FAIR? RESTORING FAIRNESS IN AXI INTERCONNECTS FOR FPGA SOCS

Francesco Restuccia, Marco Pagani, Alessandro Biondi, Mauro Marinoni, Giorgio Buttazzo - *Scuola Superiore Sant'Anna Pisa*

4A.3 ANALYTICAL PERFORMANCE MODELS FOR NOCS WITH MULTIPLE PRIORITY TRAFFIC CLASSES

Sumit K. Mandal - *Arizona State Univ.*
Raid Ayoub, MIchael Kishinevsky - *Intel Corp.*
Umit Ogras - *Arizona State Univ.*

Session 4B - CODES+ISSS: Domain Specific Optimizations

Time: 10:30 - 12:00 | Room: KC 802

Chair:

Preeti Panda - *Indian Institute of Technology, Delhi*

Co-Chair:

Ishan Thakkar - *Univ. of Kentucky*

4B.1 DMAZERUNNER: EXECUTING PERFECTLY NESTED LOOPS ON DATAFLOW ACCELERATORS

Shail Dave - *Arizona State Univ.*
Youngbin Kim - *Yonsei Univ.*
Sasikanth Avancha - *Intel Corp.*
Kyoungwoo Lee - *Yonsei Univ.*
Aviral Shrivastava - *Arizona State Univ.*

4B.2 COMPOSITIONAL DESIGN OF MULTI-ROBOT SYSTEMS CONTROL SOFTWARE ON ROS

Stefano Spellini - *Univ.' di Verona*
Michele Lora - *Singapore Univ. of Technology and Design*
Franco Fummi - *Univ.' di Verona*
Sudipta Chattopadhyay - *Singapore Univ. of Technology and Design*

4B.3 WORK-IN-PROGRESS: A SIMD-AWARE PRUNING TECHNIQUE FOR CONVOLUTIONAL NEURAL NETWORKS WITH MULTI-SPARSITY LEVELS

Jeonggyu Jang, Kyusik Choi, Hoeseok Yang - *Ajou Univ.*

4B.4 WORK-IN-PROGRESS: BPNET: BRANCH-PRUNED CONDITIONAL NEURAL NETWORK FOR SYSTEMATIC TIME-ACCURACY TRADEOFF IN DNN INFERENCE

Kyungchul Park, **Youngmin Yi** - *Univ. of Seoul*

4B.5 WORK-IN-PROGRESS: A SIMULATION FRAMEWORK FOR DOMAIN-SPECIFIC SYSTEM-ON-CHIPS

Samet Egemen Arda, Anish NK, Ahmet Alper Goksoy - *Arizona State Univ.*
Joshua Mack, Nirmal Kumbhare - *Univ. of Arizona*
Anderson Sartor - *Carnegie Mellon Univ.*
Ali Akoglu - *Univ. of Arizona*
Radu Marculescu - *Carnegie Mellon Univ.*
Umit Ogras - *Arizona State Univ.*

4B.6 WORK-IN-PROGRESS: EAST-DNN: EXPEDITING ARCHITECTURAL SIMULATIONS USING DEEP NEURAL NETWORKS

Arko Dutt - *Nanyang Technological Univ.*
Govind Narasimman, Lin Jie, Vijay Ramaseshan Chandrasekhar - *I2R, A*STAR Singapore*
Mohamed M. Sabry - *Nanyang Technological Univ.*

4B.7 WORK-IN-PROGRESS: A CONCEPT OF A HARDWARE DESIGN ENVIRONMENT WITH THE FUNCTIONAL LANGUAGE ELIXIR

Hideki Takase, Kentaro Matsui - *Kyoto Univ.*
Yoshihiro Ueno - *Delight Systems, Co., Ltd.*
Masakazu Mori - *Karabiner Technology, Inc.*
Yuki Hisae, Susumu Yamazaki - *Univ. of Kitakyushu*

** Indicates Best Paper Candidate*

Session 4C - EMSOFT: Verification and Testing

Time: 10:30 - 12:00 | Room: KC 905/907

Chair:

Renato Mancuso - *Boston Univ.*

4C.1* STATISTICAL VERIFICATION OF HYPERPROPERTIES FOR CYBER-PHYSICAL SYSTEMS

Yu Wang, Mojtaba Zarei - *Duke Univ.*
Borzoo Bonakdarpour - *Iowa State Univ.*
Miroslav Pajic - *Duke Univ.*

4C.2* POLAR: FUNCTION CODE AWARE FUZZ TESTING OF ICS PROTOCOL

Zhengxiong Luo, Feilong Zuo, Yu Jiang, Jian Gao - *Tsinghua Univ.*
Xun Jiao - *Villanova Univ.*
Jiaguang Sun - *Tsinghua Univ.*

4C.3 STRUCTURAL TEST COVERAGE CRITERIA FOR DEEP NEURAL NETWORKS

Youcheng Sun - *Univ. of Oxford*
Xiaowei Huang - *Univ. of Liverpool*
Daniel Kroening - *Univ. of Oxford*
James Sharp, Matthew Hill, Rob Ashmore - *Defence Science and Technology Laboratory*

** Indicates Best Paper Candidate*

Special Session 4D - IoMT: Cyber-Physical Monitoring, Diagnosis, Treatment Analysis, and Online Therapy

Time: 10:30 - 12:00 | Room: KC 406

Chair:

Sergio Pequito - *Rensselaer Polytechnic Institute*

Organizers:

Amir Aminifar - *École Polytechnique Fédérale de Lausanne*
Vaishnavi Ranganathan - *Microsoft Research*
James Weimer - *Univ. of Pennsylvania*
Rahul Mangharam - *Univ. of Pennsylvania*

Algorithmic and hardware developments in the area of smart sensing, modeling, analysis and actuation pave the way for advanced personalized cyber-physical (medical) diagnosis and online therapy. Towards this end, this special session will cover:

(1) We discuss the design of multi-parametric epilepsy monitoring wearables targeting to provide solutions to two fundamental problems: personalization and energy-scalability. The first problem is addressed by proposing a self-learning methodology for epileptic seizure detection that allows to perform automatic labeling of seizures in order to generate personalized training data with minimal user intervention. The second problem is tackled in epileptic seizures detection by introducing the concept of self-awareness in wearable systems monitoring the cardiac and respiratory systems of the patient in order to decrease system energy consumption and improve seizures detection quality by machine-learning model enhancement.

(2) Next, we will cover two basic challenges that we must overcome to establish a self-sufficient sensing modality for physiological monitoring. The first is with delivering power to the increasing number of sensing devices, especially when they are worn or implanted in the human body. The second is with communicating the sensed/analyzed data out of these devices efficiently. We will share the lessons learned while working on wireless biomedical implantable and wearable sensors and highlight remaining challenges.

(3) Finally, we address the personalized medicine using the internet of medical things (IoMT). Specifically, we will overview IoMT challenges and research opportunities associated with (i) collecting the right data, (ii) clinical decision support, and (iii) physiological closed-loop control. In addition, we will present some promising solutions to aspects of the aforementioned problems in the context of remotely monitoring infant hypoxemia and the artificial pancreas for Type 1 Diabetes.

4D.1 SELF-LEARNING EDGE MEDICAL SENSORS FOR PERSONALIZED AND ENERGY-SCALABLE EPILEPSY MONITORING

Amir Aminifar - *École Polytechnique Fédérale de Lausanne*

4D.2 WIRELESS BIOMEDICAL SENSING: POWER, COMPUTATION AND COMMUNICATION FOR WEARABLE AND IMPLANTABLE DEVICES

Vaishnavi Ranganathan - *Microsoft Research*

4D.3 PERSONALIZING MEDICINE IN AN IMPERSONAL WORLD: CHALLENGES AND OPPORTUNITIES IN THE INTERNET-OF-MEDICAL-THINGS

James Weimer - *Univ. of Pennsylvania*

4D.4 COMPUTER-AIDED CLINICAL TRIALS FOR IMPLANTABLE MEDICAL DEVICES: ROBUSTNESS ANALYSIS

Rahul Mangharam - *Univ. of Pennsylvania*

Poster Session

Time: 12:00 - 12:30 | Room: Eisner Lubin Auditorium

** Indicates Best Paper Candidate*

Session 5A - CASES: Emerging Technologies

Time: 13:30 - 15:00 | Room: KC 405

Chair:
Ryan Kim - *Colorado State Univ.*

5A.1 ENABLING AND EXPLOITING PARTITION-LEVEL PARALLELISM (PALP) IN PHASE CHANGE MEMORIES
Shihao Song, **Anup Das** - *Drexel Univ.*
Onur Mutlu - *ETH Zurich*
Nagarajan Kandasamy - *Drexel Univ.*

5A.2 SYNTERFACE: EFFICIENT CHIP-TO-WORLD INTERFACING FOR FLOW-BASED MICROFLUIDIC BIOCHIPS USING CONTROL-PIN MINIMIZATION
Aditya Sridhar, Mohamed Ibrahim, Krishnendu Chakrabarty - *Duke Univ.*

5A.3 WORK-IN-PROGRESS: PORTING NEW VERSATILE VIDEO CODING TRANSFORMS TO A HETEROGENEOUS GPU-BASED TECHNOLOGY
Manuel Floriano Vázquez, Anup Saha, Rafael Medina Morillas, **Miguel Chavarrías,** Fernando Pescador del Oso - *Univ. Politécnica de Madrid*

5A.4 WORK-IN-PROGRESS: MITIGATING WRITE DISTURBANCE IN PHASE CHANGE MEMORY ARCHITECTURES
Chao-Hsuan Huang, Ishan Thakkar - *Univ. of Kentucky*

5A.5 WORK-IN-PROGRESS: SEQUENCE-CRAFTER: SIDE-CHANNEL ENTROPY MINIMIZATION TO THWART TIMING-BASED SIDE-CHANNEL ATTACKS
Abhijitt Dhavlle, Sahil Bhat, Setareh Rafatirad, Houman Homayoun, Sai Manoj Pudukotai Dinakarrao - *George Mason Univ.*

5A.6 WORK-IN-PROGRESS: SAT TO SAT-HARD CLAUSE TRANSLATOR
Rakibul Hassan, Sai Manoj Pudukotai Dinkarrao, Houman Homayoun, Setareh Rafatirad - *George Mason Univ.*

5A.7 WORK-IN-PROGRESS: MICROARCHITECTURAL EVENTS AND IMAGE PROCESSING-BASED HYBRID APPROACH FOR ROBUST MALWARE DETECTION
Sanket Shukla, Gaurav Kolhe, Sai Manoj PD, Setareh Rafatirad - *George Mason Univ.*

5A.8 WORK-IN-PROGRESS: FLEXIBLE GROUP-LEVEL PRUNING OF DEEP NEURAL NETWORKS FOR FAST INFERENCE ON MOBILE GPUS
Kwangbae Lee, Hoseung Kim, Hayun Lee, Dongkun Shin - *Sungkyunkwan Univ.*

Session 5B - CODES+ISSS: Adaptive and Intermittent Embedded Systems

Time: 13:30 - 15:00 | Room: KC 802

Chair:
Andreas Gerstlauer - *Univ. of Texas, Austin*

Co-Chair:
Amlan Ganguly - *Rochester Institute of Technology*

5B.1* ACCUMULATIVE DISPLAY UPDATING FOR INTERMITTENT SYSTEMS
Hashan Roshantha Mendis, Pi-Cheng Hsiu - *Academia Sinica*

5B.2 FLORA: FLOORPLAN OPTIMIZER FOR RECONFIGURABLE AREAS IN FPGAS
Biruk B. Seyoum - *Scuola Superiore Sant'Anna*
Alessandro Biondi, Giorgio Buttazzo - *Scuola Superiore Sant'Anna*

5B.3 HESSLE-FREE: HETEROGENEOUS SYSTEMS LEVERAGING FUZZY CONTROL FOR RUNTIME RESOURCE MANAGEMENT
Kasra Moazzemi, Biswadip Maity, Saehanseul Yi, Amir M. Rahmani, Nikil Dutt - *Univ. of California, Irvine*

** Indicates Best Paper Candidate*

Session 5C - EMSOFT: Modeling and Design II

Time: 13:30 - 15:00 | Room: KC 905/907

Chair:
Marc Pouzet - *Université Pierre et Marie Curie*

5C.1 GRAPH-BASED MODELING, SCHEDULING, AND VERIFICATION FOR INTERSECTION MANAGEMENT OF INTELLIGENT VEHICLES
Yi-Ting Lin, Hsiang Hsu, Shang-Chien Lin, **Chung-Wei Lin**, Iris Hui-Ru Jiang - *National Taiwan Univ.*
Changliu Liu - *Carnegie Mellon Univ.*

5C.2 SPECIFICATION MINING AND ROBUST DESIGN UNDER UNCERTAINTY: A STOCHASTIC TEMPORAL LOGIC APPROACH
Jyotirmoy Deshmukh, Panagiotis Kyriakis, Paul Bogdan - *Univ. of Southern California*

5C.3 WORK-IN-PROGRESS: POWERMONITOR: DESIGN PATTERN FOR MODELLING ENERGY-AWARE EMBEDDED SYSTEMS
Michael Uelschen, Marco Schaarschmidt, Christian Fuhrmann, Clemens Westerkamp - *Univ. of Applied Sciences at Osnabrueck*

5C.4 WORK-IN-PROGRESS: DELAY BOUND FUNCTION FOR CYBER-PHYSICAL SYSTEMS
Akramul Azim - *Univ. of Ontario Institute of Technology*

5C.5 WORK-IN-PROGRESS: PHYSICS-BASED SOFTWARE ANALYSIS FOR SAFETY-CRITICAL EMBEDDED APPLICATIONS
Philipp Göttlich - *ETAS GmbH*
Hans-Christian Reuss - *Univ. of Stuttgart*

5C.6 WORK-IN-PROGRESS: VERIFIABLY SAFE SCUBA DIVING USING COMMODITY SENSORS
Viren Bajaj, Karim Elmaaroufi - *Carnegie Mellon Univ.*
Nathan Fulton - *Massachusetts Institute of Technology*
Andre Platzer - *Carnegie Mellon Univ.*

** Indicates Best Paper Candidate*

Special Session 5D - IoMT: Deciphering the Brain: From Mathematical Models to Computing Platforms for Cyber-Human Autonomy Symbiosis

Time: 13:30 - 15:00 | Room: KC 406

Chair:

James Weimer - *Univ. of Pennsylvania*

Organizers:

Sergio Pequito - *Rensselaer Polytechnic Institute*
Miroslav Pajic - *Duke Univ.*
Arian Ashourvan - *Penns Center for Neuroengineering and Therapeutics and the Penn Epilepsy Center, Univ. of Penns*
Partha Pratim Pande - *Washington State Univ.*

A fundamental challenge in neuroscience is to uncover the principles governing complex interactions between the brain and its external environment. The development of functional neuroimaging techniques and tools from graph theory, network science, and computational neuroscience have markedly expanded opportunities to study the intrinsic organization of brain activity. However, many current computational models are fundamentally limited by little to no explicit assessment of the brains constant and crucial interactions with external stimuli. Moreover, the complex multiscale spatiotemporal dynamics exhibited by brain activity makes the modeling, analysis and discovery of therapeutic strategies harder highlighting new challenges for Internet-of-Medical-Things targeting the brain.

To address these limitations, this special session discusses the following pioneering approaches: (1) By leveraging concepts from dynamical, control systems and fractal theories, we describe a new suite of mathematical modeling of brain activity that provides new and more efficient strategies for understanding healthy and disease regimes. We discuss the design of EEG-based non-invasive brain machine interfaces and the use of multi-dimensional fractal dynamic models for predicting the brain state for specific tasks.

(2) To treat several neurological disorders (e.g., alleviating symptoms of Parkinson's disease), we present the design of energy efficient deep brain stimulation (DBS) devices. We discuss the development of open and closed-loop DBS controllers, based on our physiological Basal Ganglia Model (BGM) and a hardware platform with a fully programable interface exposing (a) functional (continuous) electrical potentials for validation through simulation and device testing, and (b) logical signals for discrete event-based controller analysis.

(3) We discuss the joint estimation of the intrinsic organization of brain activity and extrinsic stimuli. We demonstrate the utility of this scheme by accurately estimating unknown external stimuli in a synthetic example. Next, we examine brain activity at rest and task for 99 subjects from the Human Connectome Project, and find significant task-related changes in the identified system, and task-related increases in the estimated external inputs showing high similarity to known task regressors. Together, our embodied model of brain activity provides an avenue to gain deeper insight into the relationship between cortical functional dynamics and their drivers.

(4) Finally, we describe a spatiotemporal fractal parallel algorithm to efficiently analyze brain activity data and discuss the design of a machine-learning-inspired wireless network-on-chip (WiNoC)-based manycore architecture for handling the compute- and communication-intensive nature of the brain-machine-body-interface application.

Throughout the entire special session, we will highlight numerous open mathematical, algorithmic and hardware implementation related challenges that remain to be addressed by the IoT research community.

5D.1 TOWARDS PERSONALIZED REAL-TIME CLOSED-LOOP BRAIN-MACHINE-BRAIN NEUROTECHNOLOGIES

Sergio Pequito - *Rensselaer Polytechnic Institute*

5D.2 DESIGN OF EFFICIENT DEEP BRAIN STIMULATION DEVICES

Miroslav Pajic - *Duke Univ.*

5D.3 A DYNAMICAL SYSTEMS FRAMEWORK TO UNCOVER THE DRIVERS OF LARGE-SCALE CORTICAL ACTIVITY

Arian Ashourvan - *Penns Center for Neuroengineering and Therapeutics and the Penn Epilepsy Center, Univ. of Penns*

5D.4 NETWORK-ON-CHIP-ENABLED MANYCORE ARCHITECTURES FOR BRAIN-MACHINE-INTERFACE APPLICATIONS

Partha Pande - *Washington State Univ.*

** Indicates Best Paper Candidate*

Session 6A - CASES: Embedded Systems Design

Time: 15:15 - 16:45 | Room: KC 405

Chair:
Siddharth Garg - *New York Univ.*

6A.1* OUTPUT-BASED INTERMEDIATE REPRESENTATION FOR TRANSLATION OF TEST PATTERN PROGRAMS
Minsu Kim, Jeong-keun Park - *Seoul National Univ.*
Sungyeol Kim, Insu Yang, Hyunsoo Jung - *Samsung Electronics Co., Ltd*
Soo-Mook Moon - *Seoul National Univ.*

6A.2 READY: A FINE-GRAINED MULTITHREADING OVERLAY FRAMEWORK FOR MODERN CPU-FPGA DATAFLOW APPLICATIONS
Lucas Braganca da Silva, **Ricardo Ferreira**, Michael Canesche, Marcelo de Matos Menezes, Maria Dalila Vieira, Jeronimo Costa Penha - *Univ. Federal de Vicosa*
Peter Jamieson - *Miami Univ.*
José Augusto Nacif - *Univ. Federal de Vicosa*

6A.3 MULTI-OBJECTIVE EXPLORATION FOR PRACTICAL OPTIMIZATION DECISIONS IN BINARY TRANSLATION
Sunghyun Park - *Univ. of Michigan*
Youfeng Wu, Janghaeng Lee, Amir Aupov - *Intel Corp.*
Scott Mahlke - *Univ. of Michigan*

** Indicates Best Paper Candidate*

Session 6B - CODES+ISSS: Reliability, Security, and Timing

Time: 15:15 - 16:45 | Room: KC 802

Chair:
Aviral Shrivastava - *Arizona State Univ.*

Co-Chair:
Kyoungwoo Lee - *Yonsei Univ., Seoul*

6B.1 UNIFIED TESTING AND SECURITY FRAMEWORK FOR WINOC-ENABLED MULTICORE CHIPS
Abhishek Vashist, Andrew Keats - *Rochester Institute of Technology*
Sai Manoj Pudukotai Dinakarrao - *George Mason Univ.*
Amlan Ganguly - *Rochester Institute of Technology*

6B.2 CACHE LOCKING CONTENT SELECTION ALGORITHMS FOR ARINC-653 COMPLIANT RTOS
Alexy Torres Aurora Dugo, Jean-Baptiste Lefoul, Felipe Gohring de Magalhaes, Gabriela Nicolescu - *Polytechnique Montréal*
Dahman Assal - *Mannarino Systems & Software Inc.*

6B.3 WORK-IN-PROGRESS: A SCALABLE STOCHASTIC NUMBER GENERATOR FOR PHASE CHANGE MEMORY BASED IN-MEMORY STOCHASTIC PROCESSING
Supreeth Mysore Shivanandamurthy, Ishan Thakkar, Sayed Ahmad Salehi - *Univ. of Kentucky*

6B.4 WORK-IN-PROGRESS: CACHE-AWARE DYNAMIC SKEWED TREE FOR FAST MEMORY AUTHENTICATION
Saru Vig - *Nanyang Technological Univ.*
Rohan Juneja - *Qualcomm*
Siew Kei Lam, Jiang Guiyuan - *Nanyang Technological Univ.*

6B.5 WORK-IN-PROGRESS: DEVOS: A LEARNING-BASED DELAY MODEL OF VOLTAGE-SCALED CIRCUITS
Dongning Ma - *Villanova Univ.*
Siyu Shen - *Boston Univ.*
Xun Jiao - *Villanova Univ.*

6B.6 WORK-IN-PROGRESS: MITIGATING INTER-CHANNEL CROSSTALK NON-UNIFORMITY IN MICRORING FILTER ARRAYS OF PHOTONIC NOCS
Venkata Sai Praneeth Karempudi, Ishan Thakkar - *Univ. of Kentucky*

6B.7 WORK-IN-PROGRESS: PREGC: PRE-MIGRATING VALID PAGES TO RELIEVE PERFORMANCE CLIFF OF 3D SOLID-STATE DRIVES
Yajuan Du, Wei Liu, Rui Wang, Yao Zhou - *Wuhan Univ. of Technology*
Jason Xue - *City Univ. of Hong Kong*

Session 6C - EMSOFT: Hybrid Systems

Time: 15:15 - 16:45 | Room: KC 905/907

Chair:
Xin Chen - *Univ. of Dayton*

6C.1 ROBUST REACHABLE SET: ACCOUNTING FOR UNCERTAINTIES IN LINEAR DYNAMICAL SYSTEMS
Bineet Ghosh - *Univ. of North Carolina at Chapel Hill*
Parasara Sridhar Duggirala - *Univ. of North Carolina at Chapel Hill*

6C.2 COUNTER-EXAMPLE GUIDED ABSTRACTION REFINEMENT FOR POLYHEDRAL PROBABILISTIC HYBRID SYSTEMS
Ratan Lal, Pavithra Prabhakar - *Kansas State Univ.*

6C.3 AGGREGATION STRATEGIES IN REACHABLE SET COMPUTATION OF HYBRID SYSTEMS: A SAFE SATELLITE RENDEZVOUS CASE STUDY
Parasara Sridhar Duggirala - *Univ. of North Carolina at Chapel Hill*
Stanley Bak - *United States Air Force Research Lab*

** Indicates Best Paper Candidate*

Special Session 6D - IoMT: Security, Privacy, Dependability, Reliability, and Resieliency in IoMT

Time: 15:15 - 16:45 | Room: KC 406

Chair:

Paul Bogdan - *USC*

Organizers:

Soroush Abbaspour - *IBM*
Ramesh Karri - *New York Univ.*
Kevin Fu - *Univ. of Michigan*

In this special session, we will review recent challenges concerning the security of Internet-of-Medical-Things and discuss a few hot topics such as the blockchain and biochip technologies for healthcare.

6D.1 REIMAGINING HEALTHCARE: BLOCKCHAIN AND IOT USECASES
Soroush Abbaspour - *IBM*

6D.2 CYBERPHYSICAL BIOCHIP SECURITY
Ramesh Karri - *New York, Univ.*

6D.3 CYBERSECURITY FOR MEDICAL DEVICES
Kevin Fu - *Univ. of Michigan*

Social Event

Time: 17:30 - 22:00 | Carmine's Restaurant in Times Sq & Broadway Show

The social event starts with dinner at Carmine's Restaurant in Times Sq followed by a Broadway Show.

https://www.carminesnyc.com/locations/times-square

** Indicates Best Paper Candidate*

WEDNESDAY, OCTOBER 16
SCHEDULE OF EVENTS

	KC405	KC914	KC905/907	KC406
09:00 - 10:00	**KEYNOTE**: "Cyber-Physical-Human Systems: Opportunities and Challenges", Pramod Khargonekar, UCI | Room: Eisner Lubin Auditorium			
10:00 - 10:30	**Poster Session & Coffee Break** | Room: Eisner Lubin Auditorium			
10:30 - 11:30	**CASES:** *Real-time and Secure Systems Design*	**CODES+ISSS:** *Design Space Exploration*	**EMSOFT:** *Control, Resource Allocation and Sensing*	**EMSOFT:** *Systems Software*
12:00 - 12:30	**Poster Session** | Room: Eisner Lubin Auditorium			
12:30 - 13:30	**Lunch** | Room: Eisner Lubin Auditorium			
13:30 - 15:00	**Special Session:** *Taming Extreme Heterogeneity via Machine Learning based Design of Autonomous Manycore Systems*	**CODES+ISSS:** *System Modeling and Analysis*	**EMSOFT:** *Neural Networks and Safe Autonomy*	**ACM Student Research Competition**
15:00 - 15:30	**Poster Session & Coffee Break** | Room: Eisner Lubin Auditorium			
15:30 - 17:00	**Special Session** *Analyses and Architectures for Mixed-Critical Systems: Industry Trends and Research Perspective*	**CODES+ISSS:** *IoT Systems*	**EMSOFT:** *Resource Allocation and Scheduling*	**ACM Student Research Competition**
17:00 - 17:30	**Poster Session** | Room: Eisner Lubin Auditorium			
17:30 - 18:15	**Awards Ceremony:** | Room: Eisner Lubin Auditorium			
18:15 - 19:45	**Panel: The Internet of Medical Things (IoMT): What is the Future?** Room: Eisner Lubin Auditorium			

Keynote: Cyber-Physical-Human Systems: Opportunities and Challenges

Time: 9:00 - 10:00 | Room: Eisner Lubin Auditorium

Speaker:
Pramod Khargonekar - *Univ. of California, Irvine*

Cyber-physical systems are becoming increasingly integrated into the fabric of our society. Dramatic advances in machine learning are increasing the potential capabilities of cyber-physical systems leading to the emergence of cognitive cyber-physical systems. These trends are becoming visible and even accelerating across many sectors: transportation, manufacturing, medical, agricultural. As a result, there are significant important interactions between cyber-physical systems and humans at multiple levels of organization and behavior. This range spans from individuals to companies to society as a whole. In this talk, I will share my perspective on these developments and the emerging challenges and opportunities for the research community. I will make the case that we are on the cusp of the perhaps the most significant opportunity to pursue new research advances that will benefit society, in terms of economic prosperity, health and security, by meaningfully connecting the field of cyber-physical systems with machine learning on the one hand and social-behavioral-economic sciences on the other.

Biography: Pramod Khargonekar received B. Tech. Degree in electrical engineering in 1977 from the Indian Institute of Technology, Bombay, India, and M.S. degree in mathematics in 1980 and Ph.D. degree in electrical engineering in 1981 from the University of Florida, respectively. He was Chairman of the Department of Electrical Engineering and Computer Science from 1997 to 2001 and also held the position of Claude E. Shannon Professor of Engineering Science at The University of Michigan. From 2001 to 2009, he was Dean of the College of Engineering and Eckis Professor of Electrical and Computer Engineering at the University of Florida till 2016. After serving briefly as Deputy Director of Technology at ARPA-E in 2012-13, he was appointed by the National Science Foundation (NSF) to serve as Assistant Director for the Directorate of Engineering (ENG) in March 2013, a position he held till June 2016. Currently, he is Vice Chancellor for Research and Distinguished Professor of Electrical Engineering and Computer Science at the University of California, Irvine. His research and teaching interests are centered on theory and applications of systems and control. He has received numerous honors and awards including IEEE Control Systems Award, IEEE Baker Prize, IEEE CSS Axelby Award, NSF Presidential Young Investigator Award, AACC Eckman Award, and is a Fellow of IEEE, IFAC, and AAAS.

Session 7A - CASES: Real-time and Secure Systems Design

Time: 10:30 - 12:00 | Room: KC 405

Chair:
Anup Das - *Drexel Univ.*

7A.1 END-TO-END TIMING ANALYSIS OF SPORADIC CAUSE-EFFECT CHAINS IN DISTRIBUTED SYSTEMS
Marco Dürr, Georg von der Brüggen - *Technische Univ. Dortmund*
Kuan-Hsun Chen - *Technical Univ. of Dortmund*
Jian-Jia Chen - *Technische Univ. Dortmund*

7A.2 HIGH-LEVEL SYNTHESIS OF APPROXIMATE DESIGNS UNDER REAL-TIME CONSTRAINTS
Marcos Tomazzoli Leipnitz, Gabriel Luca Nazar - *Univ. Federal do Rio Grande do Sul*

7A.3 LOCKING THE DESIGN OF BUILDING BLOCKS FOR QUANTUM CIRCUITS
Samah Saeed - *City College of New York*
Robert Wille - *Johannes Kepler Univ. Linz*
Ramesh Karri - *New York Univ.*

Session 7B - CODES+ISSS: Design Space Exploration

Time: 10:30 - 12:00 | Room: KC 914

Chair:
Kyuongwoo Lee - *Yonsei Univ.*

Co-Chair:
Radu Marculescu - *Carnegie Mellon Univ.*

7B.1 MOOS: A MULTI-OBJECTIVE DESIGN SPACE EXPLORATION AND OPTIMIZATION FRAMEWORK FOR NOC ENABLED MANYCORE SYSTEMS
Aryan Deshwal, Nitthilan Kannappan Jayakodi, Biresh Kumar Joardar, **Jana Doppa**, Partha Pratim Pande - *Washington State Univ.*

7B.2 IGOR, GET ME THE OPTIMUM! PRIORITIZING IMPORTANT DESIGN DECISIONS DURING THE DSE OF EMBEDDED SYSTEMS
Fedor Smirnov, Behnaz Pourmohseni - *Friedrich-Alexander - Univ. Erlangen-Nürnberg*
Michael Glaß - *Ulm Univ.*
Jürgen Teich - *Univ. Erlangen-Nürnberg*

7B.3 WORK-IN-PROGRESS: DESIGN SPACE EXPLORATION OF MULTI-TASK PROCESSING ON SPACE SHARED FPGAS
Umar Minhas, Roger Woods, Georgios Karakonstantis - *Queens Univ. Belfast*

7B.4 WORK-IN-PROGRESS: OFFLOADING CACHE CONFIGURATION PREDICTION TO AN FPGA FOR HARDWARE SPEEDUP AND OVERHEAD REDUCTION
Ruben Vazquez, Ann Gordon-Ross, Greg Stitt - *Univ. of Florida*

7B.5 WORK-IN-PROGRESS: A CASE FOR DESIGN SPACE EXPLORATION OF CONTEXT-AWARE ADAPTIVE EMBEDDED SYSTEMS
Rajesh Kedia, M. Balakrishnan, Kolin Paul - *Indian Institute of Technology Delhi*

7B.6 WORK-IN-PROGRESS: DRAMA: A HIGH EFFICIENT NEURAL NETWORK ACCELERATOR ON FPGA USING DYNAMIC RECONFIGURATION
Yang Yang, Chao Wang, Xuehai Zhou - *Univ. of Science and Technology of China*

7B.7 WORK-IN-PROGRESS: VIDEO ANALYTICS FROM EDGE TO SERVER
Jiashen Cao, Ramyad Hadidi, Joy Arulraj, Hyesoon Kim - *Georgia Institute of Technology*

** Indicates Best Paper Candidate*

Session 7C - EMSOFT: Control, Resource Allocation and Sensing

Time: 10:30 - 12:00 | Room: KC 905/907

Chair:

Shan Lin - *Stony Brook Univ.*

7C.1 MEMORY-EFFICIENT MIXED-PRECISION IMPLEMENTATIONS FOR ROBUST EXPLICIT MODEL PREDICTIVE CONTROL

Mahmoud Salamati - *Max Planck Institute*
Rocco Salvia - *Univ. of Utah*
Eva Darulova - *Max Planck Institute*
Sadegh Soudjani - *Newcastle Univ.*
Rupak Majumdar - *Max Planck Institute*

7C.2 NUMERICAL REPRESENTATION OF DIRECTED ACYCLIC GRAPHS FOR EFFICIENT DATAFLOW EMBEDDED RESOURCES ALLOCATION

Florian Arrestier, Karol Desnos - *Univ Rennes*
Eduardo Juarez - *Univ. Politecnica de Madrid*
Daniel Menard - *Univ Rennes*

7C.3 WORK-IN-PROGRESS: ACHAL: BUILDING HIGHLY RELIABLE NETWORKED CONTROL SYSTEMS

Arpan Gujarati - *Max Planck Institute for Software Systems*
Malte Appel - *Saarland Univ.*
Björn Brandenburg - *Max Planck Institute for Software Systems*

7C.4 WORK-IN-PROGRESS: A NEUROMORPHIC APPROACH OF THE SOUND SOURCE LOCALIZATION TASK IN REAL-TIME EMBEDDED SYSTEMS

Daniel Gutierrez-Galan, Juan Pedro Dominguez-Morales, Angel Jimenez-Fernandez, Ricardo Tapiador-Morales, Antonio Rios-Navarro, Alejandro Linares-Barranco - *Univ. of Seville*

7C.5 WORK-IN-PROGRESS: PRIVATE RUNTIME VERIFICATION

Houssam Abbas - *Oregon State Univ.*

7C.6 WORK-IN-PROGRESS: COMMUNICATION AND SECURITY TRADE-OFFS FOR WEARABLE MEDICAL SENSOR SYSTEMS IN HOSPITALS

Jori Winderickx - *Katholieke Univ. Leuven*
Pierre Bellier - *Univ. of Liege*
Patrick Duflot - *Centre Hospitalier Univ. de Liège*
Dorothée Coppieters - *Univ. of Liege*
Nele Mentens - *Katholieke Univ. Leuven*

** Indicates Best Paper Candidate*

Session 7D - EMSOFT: Systems Software

Time: 10:30 - 12:00 | Room: KC 406

Chair:

Alessandro Biondi - *Scuola Superiore Sant'Anna - Pisa*

7D.1 HONEY, I SHRUNK THE ELFS: LIGHTWEIGHT BINARY TAILORING OF SHARED LIBRARIES

Andreas Ziegler, Julian Geus, Bernhard Heinloth, Timo Hönig - *Friedrich-Alexander-Univ. Erlangen-Nürnberg*
Daniel Lohmann - *Leibniz Univ. Hannover*

7D.2 MXU: TOWARDS PREDICTABLE, FLEXIBLE, AND EFFICIENT MEMORY ACCESS CONTROL FOR THE SECURE IOT

Runyu Pan, Gabriel Parmer - *George Washington Univ.*

7D.3 TREBLE: FAST SOFTWARE UPDATES BY CREATING AN EQUILIBRIUM IN AN ACTIVE SOFTWARE ECOSYSTEM OF GLOBALLY DISTRIBUTED STAKEHOLDERS

Keun Soo Yim, Iliyan Malchev, Andrew Hsieh, Dave Burke - *Google*

Poster Session

Time: 12:00 - 12:30 | Room: Eisner Lubin Auditorium

ACM Student Research Competition

Time: 13:30 - 15:00 | Room: KC 406

Organizers:

Renato Mancuso - *Boston Univ.*
Hyoseung Kim - *Univ. of California, Riverside*

** Indicates Best Paper Candidate*

Special Session 8A: Taming Extreme Heterogeneity via Machine Learning based Design of Autonomous Manycore Systems

Time: 13:30 - 15:00 | Room: KC 405

Chair:
Siddharth Garg - *NYU*

Organizers:
Hai (Helen) Li - *Duke Univ.*
Janardhan Rao Doppa - *Washington State Univ.*
Paul Bogdan - *Univ. of Southern California*

The end of lithographic and exponential clock frequency scaling call for developing new programming models and self-optimizing strategies to discover the optimal degree of parallelization at runtime from old codes while seeing new data and take advantage of extreme heterogeneity (EH). Avoiding data movement requires in situ computing where data resides, and exploiting EH in emerging processing, communication, and memory technologies. The broad topic of extreme heterogeneity, programming models and design methodologies for autonomous massive manycore chips is actively pursued by a number of researchers worldwide, from a variety of different perspectives. Successful solutions will likely lead to a new computing paradigm that goes well beyond von-Neuman architectures and enable the design of self-programming and self-optimizing computing systems. In this special session, we will discuss the theoretical and algorithmic foundations for designing autonomous massive manycore platforms by considering the extreme heterogeneity in processing, communication and memory, the challenges of design space exploration and optimization, and appropriate programming models.

8A.1 PROCESS-IN-MEMORY ARCHITECTURE DESIGN AND OPTIMIZATION FOR DEEP LEARNING APPLICATIONS
Hai (Helen) Li - *Duke Univ.*

8A.2 DESIGN SPACE EXPLORATION AND OPTIMIZATION METHODOLOGIES FOR HETEROGENEOUS MANYCORE SYSTEMS
Janardhan Rao Doppa - *Washington State Univ.*

8A.3 NOVEL PROGRAMMING MODELS AND ALGORITHMIC FOUNDATIONS FOR DESIGNING SELF-PROGRAMMABLE HETEROGENEOUS COMPUTING ARCHITECTURES
Paul Bogdan - *Univ. of Southern California*

Session 8B - CODES+ISSS: System Modeling and Analysis

Time: 13:30 - 15:00 | Room: KC 914

Chair:
Ishan Thakkar - *Univ. of Kentucky*

8B.1 ANALYZING VARIABLE ENTANGLEMENT FOR PARALLEL SIMULATION OF SYSTEMC TLM-2.0 MODELS
Zhongqi Cheng, Rainer Doemer - *Univ. of California, Irvine*

8B.2 EFFICIENT TRACING METHODOLOGY USING THE MICRON AUTOMATA PROCESSOR
Minjun Seo, Fadi Kurdahi - *Univ. of California, Irvine*

8B.3 ALLERIA: AN ADVANCED MEMORY ACCESS PROFILING FRAMEWORK
Hadi Brais, Preeti Ranjan Panda - *Indian Institute of Technology Delhi*

** Indicates Best Paper Candidate*

Session 8C - EMSOFT: Neural Networks and Safe Autonomy

Time: 13:30 - 15:00 | Room: KC 905/907

Chair:

Susmit Jha - *SRI International*

8C.1 SAFETY VERIFICATION OF CYBER-PHYSICAL SYSTEMS WITH REINFORCEMENT LEARNING CONTROL

Dung Tran, Feiyang Cei, Manzanas Lopez Diego, Patrick Musau, Taylor T Johnson, Xenofon Koutsoukos - *Vanderbilt Univ.*

8C.2 REACHNN: REACHABILITY ANALYSIS OF NEURAL-NETWORK CONTROLLED SYSTEMS

Chao Huang - *Northwestern Univ.*
Jiameng Fan, Wenchao Li - *Boston Univ.*
Xin Chen - *Univ. of Dayton*
Qi Zhu - *Northwestern Univ.*

8C.3 WORST-CASE SATISFACTION OF STL SPECIFICATIONS USING FEEDFORWARD NEURAL NETWORK CONTROLLERS: A LAGRANGE MULTIPLIERS APPROACH

Shakiba Yaghoubi, Georgios Fainekos - *Arizona State Univ.*

Poster Session & Coffee Break

Time: 15:00 - 15:30 | Room: Eisner Lubin Auditorium

ACM Student Research Competition

Time: 15:30 - 17:00 | Room: KC 406

Organizers:

Renato Mancuso - *Boston Univ.*
Hyoseung Kim - *Univ. of California, Riverside*

** Indicates Best Paper Candidate*

Special Session 9A: Analyses and Architectures for Mixed-Critical Systems: Industry Trends and Research Perspective

Time: 15:30 - 17:00 | Room: KC 405

Chair:

Lars Bauer - *Karlsruhe Institute of Technology*

Organizers:

Giorgio Buttazzo - *Scuola Superiore Sant'Anna of Pisa*
Jörg Henkel - *Karlsruhe Institute of Technology*
Dirk Ziegenbein - *Robert Bosch GmbH*

The ongoing Cyber-Physical Systems (CPS) and Internet of Things (IoT) revolution is leading to the ubiquity of applications with real-time requirements. Examples are smart grids, automated driving, collaborative robots, and many more. While in traditional real-time applications dedicated systems were built for each safety-critical functionality, this paradigm no longer suits emerging applications. The reason is that apart from traditional real-time requirements like a guaranteed worst-case execution time (WCET), tremendous performance requirements need to be fulfilled under additional non-functional constraints like power consumption, cost, space and weight. To fulfill these requirements, integrated mixed-criticality systems are designed instead of a dedicated system for each functionality. This integration entails that safety-critical tasks of one functionality are no longer run in isolation, but rather they share the same computing platform with low-critical or even non-critical software. A prime example of a domain that is currently undergoing the radical shift from the design of numerous isolated safety-critical systems to integrated mixed-criticality systems is the automotive industry. Where traditional automotive architectures consist of more than 100 single-function electronic control units, the industry is now moving to more centralized computing platforms. Thus, a heterogeneous mix of applications with different models of computation and with diverse requirements in terms of timing and safety criticality is run on hardware platforms that are increasingly heterogeneous, including specialized hardware accelerators, e.g., for deep learning.

When falling for old habits and designing mixed-critical systems with numerous fixed and single-function accelerators, however, the system becomes inflexible while the non-functional constraints are not fulfilled effectively. Instead, this special session will present ways to achieve the performance of application-specific accelerators while maintaining the system's flexibility using runtime reconfiguration. The crux of runtime reconfiguration in mixed-critical system design is to unite a changing set of specialized hardware accelerators, which are shared between tasks of different criticality, with WCET and schedulability guarantees without compromising performance benefits.

This special session will target this problem from two directions: (i) real-time analysis and predictable run-time mechanisms, and (ii) hardware architectures. It will further highlight how advances in one direction lead to opportunities and challenges in the other. From this context, this special session will address the vast opportunities and challenges of major architectural trends like heterogeneous multi-processor system-on-chips in the design of mixed-critical systems. This special session will benefit Univ. researchers/professors, students, industry professionals, and computing system designers who are interested in working on mixed-critical systems. And clearly, in the light of the increasing industrial demand and academic advances, this is an excellent time to revisit mixed-critical systems design in a special session.

9A.1 MIXED-CRITICALITY SYSTEMS IN PRACTICE: STATUS & CHALLENGES

Dirk Ziegenbein, Arne Hamann - *Robert Bosch GmbH*

9A.2 DEVELOPMENT AND ANALYSIS OF REAL-TIME APPLICATIONS ON HETEROGENEOUS FPGA-BASED SOC

Alessandro Biondi, Giorgio Buttazzo - *Scuola Superiore Sant'Anna of Pisa*

9A.3 RUNTIME-RECONFIGURABLE ARCHITECTURES FOR WCET GUARANTEES AND MIXED CRITICALITY

Lars Bauer, Marvin Damschen, Jörg Henkel - *Karlsruhe Institute of Technology*

* *Indicates Best Paper Candidate*

Session 9B - CODES+ISSS: Machine Learning for IoT

Time: 15:30 - 17:00 | Room: KC 914

Chair:

Sai Manoj Pudukotai Dinakarrao - *George Mason Univ.*

Co-Chair:

Fadi Kurdahi - *Univ. of California, Irvine*

9B.1 MEMORY- AND COMMUNICATION-AWARE MODEL COMPRESSION FOR DISTRIBUTED DEEP LEARNING INFERENCE ON IOT

Kartikeya Bhardwaj, Chingyi Lin, Anderson Luiz Sartor, Radu Marculescu - *Carnegie Mellon Univ.*

9B.2 QUALITY/LATENCY-AWARE REAL-TIME SCHEDULING OF DISTRIBUTED STREAMING IOT APPLICATIONS

Kamyar Mirzazad Barijough, Zhuoran Zhao, Andreas Gerstlauer - *Univ. of Texas at Austin*

9B.3 WORK-IN-PROGRESS: COOPERATIVE COMMUNICATION BETWEEN TWO TRANSIENTLY POWERED SENSORS BY REINFORCEMENT LEARNING

Yawen Wu, Zhenge Jia - *Univ. of Pittsburgh*
Fei Fang - *Carnegie Mellon Univ.*
Jingtong Hu - *Univ. of Pittsburgh*

9B.4 WORK-IN-PROGRESS: Q-LEARNING BASED ROUTING FOR TRANSIENTLY POWERED WIRELESS SENSOR NETWORK

Zhenge Jia, Yawen Wu, Jingtong Hu - *Univ. of Pittsburgh*

9B.5 WORK-IN-PROGRESS: DORY: LIGHTWEIGHT MEMORY HIERARCHY MANAGEMENT FOR DEEP NN INFERENCE ON IOT ENDNODES

Alessio Burrello - *Univ. of Bologna*
Francesco Conti - *ETH Zurich*
Angelo Garofalo, Davide Rossi - *Univ. of Bologna*
Luca Benini - *ETH Zurich*

9B.6 WORK-IN-PROGRESS: A DISTRIBUTED SMART CAMERA APPARATUS TO ENABLE SCENE IMMERSION

Erman Nghonda Tchinda, Danielle Tchuinkou Kwadjo, **Christophe Bobda** - *Univ. of Florida*

9B.7 WORK-IN-PROGRESS: AN IMPROVED NETWORK INTERFACE CARD WITH QUERY FILTER FOR BIG DATA SYSTEMS

Jinyu Zhan, Ying Li, Wei Jiang, Junting Wu - *Univ. of Electronic Science and Technology of China*
Jianping Zhu - *Tencent Technology Shenzhen Co., Ltd*

Session 9C - EMSOFT: Resource Allocation and Scheduling

Time: 15:30 - 17:00 | Room: KC 905/907

Chair:

Wolfgang Schröder-Preikschat - *Friedrich-Alexander-Universität (FAU)*

This session will focus on Resource Allocation and Scheduling Papers

9C.1 CODE-INHERENT TRAFFIC SHAPING FOR HARD REAL-TIME SYSTEMS

Dominic Oehlert, Selma Saidi, Heiko Falk - *Hamburg Univ. of Technology*

9C.2 TECHNIQUES AND ANALYSIS FOR MIXED-CRITICALITY SCHEDULING WITH MODE-DEPENDENT SERVER EXECUTION BUDGETS

Muhammad Ali Awan, Konstantinos Bletsas - *CISTER Research Centre*
Pedro Souto - *Univ. of Porto*
Benny Akesson - *Netherlands Organisation for Applied Scientific Research*
Eduardo Tovar - *CISTER Research Centre*

9C.3 PARAMETRIC SCHEDULER CHARACTERIZATION

Joost van Pinxten, Marc Geilen, Twan Basten - *Eindhoven Univ. of Technology*

** Indicates Best Paper Candidate*

Poster Session
Time: 17:00 - 17:30 | Room: Eisner Lubin Auditorium

Awards Ceremony
Time: 17:30 - 18:15 | Room: Eisner Lubin Auditorium

Panel: The Internet of Medical Things (IoMT): What is the Future?
Time: 18:15 - 19:45 | Room: Eisner Lubin Auditorium

Moderators:

Laura Pozzi - *Università della Svizzera italiana (USI)*
Amir Aminifar - *École Polytechnique Fédérale de Lausanne*

The Internet of Medical Things (IoMT) paves the foundations for intelligent and reliable personalized precision medicine. Grounded in the mathematical and physical modeling of human anatomy and physiology, it offers accurate multiscale medical monitoring through smart sensing, enabling contin-uous diagnosis via on-fly communication with medical experts. It provides hyperspectral and hyperdimensional processing and restores health through patient-specific actuation. This panel in the context of IoMT presents a complete set of industrial and academic experts to discuss with the ESWEEK atteendes about their view on the academic and industral context for the future of this topic to develop a fully-functional personalized medicine context in the IoT era.

Panelists:

Mario Konijnenburg - *IMEC - The Netherlands*
Philippe Ryvlin - *Univ. Hospital Lausanne (CHUV), Dept. of Clinical Neuroscience*
Vaishnavi Ranganathan - *Microsoft Research*
Vijay Narayanan - *Penn State Univ.*
Mudhakar Srivatsa - *IBM T.J. Watson Research Center*

** Indicates Best Paper Candidate*

WORKSHOP SCHEDULE

NYU Center for CyberSecurity, 370 Jay Street, Brooklyn, NY

THURSDAY

AAIEA: Workshop Accelerating Artificial Intelligence for Embedded Autonomy
Thursday, October 17 | Time: 09:00 - 17:00 | Room: 1017 (370 Jay St. Brooklyn)

CyberCardia Medical CPS Workshop
Thursday, October 17 | Time: 09:00 - 17:30 | Room: 1012 (370 Jay St. Brooklyn)

EWiLi: Embedded Operating Systems Workshop
Thursday, October 17 | Time: 09:00 - 17:00 | Room: 1078 (370 Jay St. Brooklyn)

HENP: Workshop on Highly Efficient Neural Processing
Thursday, October 17 | Time: 09:00 - 17:00 | Room: 1013 (370 Jay St. Brooklyn)

INTESA: INTelligent Embedded Systems Architectures and Applications Workshop
Thursday, October 17 | Time: 09:00 - 17:00 | Room: 1038 (370 Jay St. Brooklyn)

THURSDAY & FRIDAY

CyPhy/WESE: Workshop on Model-Based Design of Cyber Physical Systems, and Workshop on Embedded Systems Education
Thursday, October 19 - Friday, October 20 | Room: 1014 (370 Jay St. Brooklyn)

RSP: Workshop on Rapid System Prototyping
Thursday, October 19 - Friday, October 20 | Room: 370 Jay St. 1015

SYMPOSIA SCHEDULE

THURSDAY & FRIDAY

NOCS: 12th International Symposium on Networks-on-Chip
Thursday, October 17 - Friday, October 18 | Room: NYU AD Building

AAIEA Workshop: Accelerating Artificial Intelligence for Embedded Autonomy

Time: 9:00 - 17:00 | Room: 1017 (370 Jay St. Brooklyn)

Organizers:

Alessandro Pinto - *United Technologies Research Center*
Gerald Wang - *United Technologies Research Center*
Luca Carloni - *Columbia Univ.*

The Workshop on Accelerating Artificial Intelligence for Embedded Autonomy aims at gathering researchers and practitioners in the fields of autonomy, automated reasoning, planning algorithms, and embedded systems to discuss the development of novel hardware architectures that can accelerate the wide variety of AI algorithms demanded by advanced autonomous and intelligent systems. Topics of interest include hardware architectures and design methodologies to accelerate: Applications based on deep learning, skill-level and instinctive autonomy based on deep reinforcement learning, storage and retrieval of facts in knowledge bases, logical reasoning methods such as deduction, search for classical planning algorithms and Hierarchical Task Networks (HTN), inference in probabilistic models such as Bayesian networks and probabilistic logic, planning algorithms for Markov Decision Processes (MDP), and planning algorithms for Partial Observable Markov Decision Processes (POMDP).

CyberCardia Medical CPS Workshop

Time: 9:00 - 17:30 | Room: 1012 (370 Jay St. Brooklyn)

Organizers:

Scott A. Smolka - *Stony Brook Univ.*
Rahul Mangharam - *Univ. of Pennsylvania*
Oleg Sokolsky - *Univ. of Pennsylvania*
Samuel Huang - *Univ. of Maryland, College Park*

The CyberCardia Medical CPS workshop brings together researchers with a strong interest and background in cyber-physical systems (CPS). This one-day workshop is a capstone event for the NSF-funded CPS Frontier project, CyberCardia, which involves seven universities and centers. CyberCardia researchers conduct cross-disciplinary collaborative research to radically accelerate the pace of medical-device innovation, especially in the sphere of cardiac-device design.

EWiLi: Embedded Operating Systems Workshop

Time: 9:00 - 17:00 | Room: 1078 (370 Jay St. Brooklyn)

The Embedded Operating Systems Workshop (EWiLi) aims at presenting state-of-the-art research, experimentation, significant and original realizations that focus on the design and implementation of embedded operating systems in both academic and industrial worlds. Originally focusing on embedded Linux, the "Embed With Linux" (EWiLi) workshop has since then evolved to consider embedded operating systems in general.

Program Committee Chairs:

Gedare Bloom - *Univ. of Colorado at Colorado Springs*

Dionisio De Niz - *SEI Carnegie Mellon Univ.*

Steering Committee:

Jalil Boukhobza - *Lab-STICC/Univ. Western Brittany*

Marco D. Santambrogio - *Politecnico di Milano*

Frank Singhoff - *Lab-STICC/Univ. Western Brittany*

Web and Publication Chair:

Pierre Olivier - *Virginia Tech*

HENP: Workshop on Highly Efficient Neural Processing

Time: 9:00 - 17:00 | Room: 1013 (370 Jay St. Brooklyn)

Organizers:

Yiran Chen - *Duke Univ.*

Sungjoo Yoo - *Seoul National Univ.*

The International Workshop on Highly Efficient Neural Processing is a forum for presentations of state-of-the-art research in highly efficient neural processing. The workshop will combine both oral presentations and posters, which include invited talks from Facebook, Samsung Electronics, etc.

INTESA: INTelligent Embedded Systems Architectures and Applications Workshop

Time: 9:00 - 17:00 | Room: 1038 (370 Jay St. Brooklyn)

Organizers:

Maurizio Martina - *Politecnico di Torino*
William Fornaciari - *Politecnico di Milano*

The INTESA workshop aims to give an up-to-date picture of intelligent embedded systems architectures and applications with emphasis on Smart IoT and Cyber Physical Systems, including hot topics such as accelerating deep learning. The workshop covers several aspects, from the hardware related ones to embedded software and application issues, being complementary to most of the topic addressed during the ESWEEK. From the market standpoint, scientific progress in this field are considered crucial to fuel a widespread diffusion of the potential benefits offered by the Industry 4.0 perspective. The goal of the event is to create cross-fertilization of ideas between application developers and platform providers with the participation of a mix between academic and industry people.

CyPhy/WESE: Workshop on Model-Based Design of Cyber Physical Systems, and Workshop on Embedded Systems Education

Time: 9:00 - 17:00 on Thursday | 9:00 - 13:30 on Friday | Room: 1014 (370 Jay St. Brooklyn)

Organizers:

Walid Taha - *Halmstad Univ.*
Martin Törngren - *KTH Royal Institute of Technology*

CyPhy: Cyber-physical systems (CPSs) combine computing and networking power with physical components. They enable innovation in a wide range of domains including robotics; smart homes, vehicles, and buildings; medical implants; and future-generation sensor networks. CyPhy'19 brings together researchers and practitioners working on modeling, simulation, and evaluation of CPS, based on a broad interpretation of these areas, to collect and exchange expertise from a diverse set of disciplines. The workshop places particular focus on techniques and components to enable and support virtual prototyping and testing.

WESE: The WESE workshop series aims to bring researchers, educators, and industrial representatives together to assess needs and share design, research, and experiences in embedded and cyber-physical systems education. WESE addresses questions such as "What skills and capabilities are required by the engineers of tomorrow", "How should the corresponding educational programs be formed", and "How can effective pedagogic methods be introduced in this domain"?

RSP: Workshop on Rapid System Prototyping

Time: 9:00 - 17:00 on Thursday | 9:00 - 13:30 on Friday | Room: 1015 (370 Jay St. Brooklyn)

The International Workshop on Rapid System Prototyping (RSP) emphasizes design experience sharing and collaborative approach between hardware and software research communities from industry and academy. It considers prototyping as an iterative design approach for embedded hardware and software systems. The RSP series of workshop aim at bridging the gaps in embedded system design between applications, architectures, tools, and technologies to achieve rapid system prototyping of emerging software and hardware systems.

Rapid System Prototyping workshop seeks original contributions related to this target, encompassing a wide scope ranging from formal methods for the verification of software and hardware systems to case studies of emerging embedded systems and technologies. The workshop proposes a two-day inspiring international forum for discussing the latest related innovations and research activities. The workshop program will include keynote speeches and technical papers on timely topics.

General Chairs:
Frédéric Rousseau - TIMA, *Univ. Grenoble-Alpes*
Kenneth Kent - *Univ. of New Brunswick*

Program Chairs:
Brett H. Meyer - *McGill Univ.*
Fabiano Hessel - *PUCS, BR*

International Symposium on Networks-on-Chip (NOCS)

Time: 9:00 - 17:00 | Room: NYU AD Building

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, chip-scale, and multichip package-scale communication technology, architecture, design methods, applications and systems.

NOCS brings together scientists and engineers working on NoC innovations and applications from inter-related research communities, including computer architecture, networking, circuits and systems, packaging, embedded systems, codesign, and design automation.

2019 General Chairs
Paul Bogdan - *Univ. of Southern California*
Cristina Silvano - *Politecnico di Milano*

2019 Technical Program Chairs:
Sudeep Pasricha - *Colorado State Univ.*
Ajay Joshi - *Boston Univ.*

NOCS SYMPOSIUM

THURSDAY OCT 17, 2019

[09:00 – 09:15] Opening Remarks

[09:15 – 10:15] Keynote 1

Session Chair: Sudeep Pasricha, *Colorado State Univ.*

Interconnect Meets Architecture: On-Chip Communication in the Age of Heterogeneity
Partha Pratim Pande, *Washington State Univ.*

[10:15 – 10:45] Coffee Break

[10:45 – 12:00] Regular Paper Session I: NoC and Router Design

Session Chair: Andreas Herkersdorf, *Technical Univ. of Munich*

UBERNoC: Unified Buffer Energy-Efficient Router for Network-on-Chip
Hossein Farrokhbakht, Henry Kao and Natalie Enright Jerger, *Univ. of Toronto*

Ghost Routers: Energy-Efficient Asymmetric Multicore Processors with Symmetric NoCs
Hyojun Son, *KAIST*, Hanjoon Kim, *Furiosa A.I.,* Hao Wang, *Univ. of Wisconsin-Madison*, Nam Sung Kim, *Samsung Electronics,* and John Kim, *KAIST*

BINDU: Deadlock-Freedom with One Bubble in the Network
Mayank Parasar and Tushar Krishna, *Georgia Institute of Technology*

[12:00 – 12:30] Invited Talk

Session Chair: Ajay Joshi, *Boston Univ.,*

Accelerator Fabric in Facebook Zion Training System
John Kim, *KAIST/Facebook*

[12:30 – 14:00] Lunch

[14:00 – 15:15] Special Session 1: Interconnection Networks for Deep Neural Networks

Session Chair: Tushar Krishna, *Georgia Institute of Technology*

Session Organizers: Kun-Chih (Jimmy) Chen, *National Sun Yat-sen Univ.,* Masoumeh (Azin) Ebrahimi, *KTH Royal Institute of Technology*

NoC-based DNN Accelerator: A Future Design Paradigm
Kun-Chih Chen, *National Sun Yat-sen Univ.,* Masoumeh Ebrahimi, *KTH Royal Institute of Technology*, Ting-Yi Wang, *National Sun Yat-sen Univ.,* and Yuch-Chi Yang, *National Sun Yat-sen Univ.*

Energy-Efficient and High-Performance NoC Architecture and Mapping Solution for Deep Neural Networks
Md Farhadur Reza and Paul Ampadu, *Virginia Polytechnic Institute and State Univ.*

Flow mapping and data distributing on mesh-based deep learning accelerator
Seyedeh Yasaman Hosseini Mirmahaleh, Islamic Azad *Univ., Tehran,* Midia Reshadi, *Islamic Azad Univ., Tehran*, Hesam Shabani, *Lehigh Univ.*, Xiaochen Guo, *Lehigh Univ.,* and Nader Bagherzadeh, *Univ. of California, Irvine*

[15:15 – 15:30] Lightening Talks for Work in Progress (WIP) Posters

Session Chair: Sudeep Pasricha, Colorado State Univ.,

Reinforcement Learning based Interconnection Routing and Adaptive Traffic Optimization

Sheng-Chun Kao, *Georgia Institute of Technology,* Chao-Han Huck Yang, *Georgia Institute of Technology,* Pin-Yu Chen, *IBM Watson AI Foundation Group*, Xiaoli Ma, *Georgia Institute of Technology,* and Tushar Krishna, *Georgia Institute of Technology*.

Power efficient Photonic Network-on-Chip for a Scalable GPU
Janibul Bashir, Khushal Sethi and Smruti R. Sarangi, *Indian Institute of Technology, Delhi*

CDMA-based Multiple Multicast Communications on WiNOC for efficient parallel computing
Navonil Chatterjee, *Lab-STICC, Université Bretagne Sud,* Hemanta Kumar Mondal, NIT Durgapur, Rodrigo Cataldo, *Lab-STICC, Université Bretagne Sud,* and Jean-Philippe Diguet, *Lab-STICC, Université Bretagne Sud*

Channel Mapping Strategies for Effective Protection Switching in Fail-Operational Hard Real-Time NoCs
Max Koenen, Nguyen Anh Vu Doan, Thomas Wild and Andreas Herkersdorf, *Technical Univ. of Munich*

Multi-Carrier Direct Sequence Spread Spectrum Transceiver for WiNoC
Joel Ortiz Sosa, *Univ. Rennes*, Inria, Olivier Sentieys, *Univ. Rennes*, Inria, Christian Roland, *Lab-STICC, Université Bretagne Sud,* and Cedric Killian, *Univ. Rennes, Inria*

Detection and Prevention Protocol for Black Hole Attack in Network-on-Chip
Luka Daoud and Nader Rafla, *Boise State Univ.*

Analyzing Networks-on-Chip based Deep Neural Networks
Maurizio Palesi, *Univ. of Catania*, Giuseppe Ascia, *Univ. of Catania*, Davide Patti, *Univ. of Catania*, Salvatore Monteleone, *Univ. of Catania*, Vincenzo Catania, *Univ. of Catania*, and John Jose, *Indian Institute of Technology Guwahati*

NOCS SYMPOSIUM

THURSDAY OCT 17, 2019

[15:30 – 16:15] WIP Posters and Coffee Break

[16:15 – 17:30] Regular Paper Session 2: Best Paper Nominees

Session Chair: Paul Ampadu, *Virginia Polytechnic Institute and State Univ.*

NoC-enabled Software/Hardware Co-Design Framework for Accelerating k-mer Counting
Biresh Kumar Joardar, Washington State Univ., Priyanka Ghosh, Washington State Univ., Partha Pratim Pande, Washington State Univ., Ananth Kalyanaraman, Washington State Univ., and Sriram Krishnamoorthy, Pacific Northwest National Laboratory

SMART++: Reducing cost and improving efficiency of multi-hop bypass in NoC routers
Iván Pérez, Enrique Vallejo and Ramón Beivide, Univ. of Cantabria, Santander

APEC: Improved Acknowledgement Prioritization through Erasure Coding in Bufferless NoCs
Michael Vonbun, Adrian Schiechel, Nguyen Anh Vu Doan, Thomas Wild and Andreas Herkersdorf, Technical Univ. of Munich

[19:00 – 21:00] Dinner (TBD)

FRIDAY OCT 18, 2019

[09:00 – 10:00] Keynote 2

Session Chair: Ajay Joshi, *Boston Univ.*

Toward Fast Analysis and Exploration of Communication Fabrics
Raid Ayoub, *Intel*

[10:00 – 10:15] Coffee Break

[10:15 – 11:30] Tutorial 1: System on Package (SoP): A Holistic Approach for System Integration

Session Chair: Tushar Krishna, *Georgia Institute of Technology*

Speakers: Madhavan Swaminathan, Mohan Kathaperumal, *Georgia Institute of Technology*

[11:30 – 12:30] Tutorial 2: High Performance Networks

Session Chair: Ishan Thakkar, *Univ., of Kentucky*

Engineering a specialized, high-performance network
Brian Towles, Brian Greskamp, *D.E. Shaw Research*

[12:30 – 14:00] Lunch

[14:00 – 15:40] Regular Paper Session 3: NoC Potpourri

Session Chair: Maurizio Palesi, *Univ., of Catania*

ClusCross: A New Topology for Silicon Interposer-Based Network-on-Chip
Hesam Shabani and Xiaochen Guo, Lehigh Univ.,

Distributed SDN Architecture for NoC-based Many-core SoCs
Marcelo Ruaro, PUCRS, Nedison Velloso, PUCRS, Axel Jantsch, TU Wien, Vienna, and Fernando Moraes, PUCRS

Approximate Nanophotonic Interconnects
Jaechul Lee, Univ Rennes, Inria, Cédric Killian, Univ. Rennes, Inria, Sébastien Le Beux, Concordia Univ., and Daniel Chillet, Univ Rennes, Inria

Direct-Modulated Optical Networks for Interposer Systems
Mohammad Reza Jokar, Univ., of Chicago, Lunkai Zhang, Univ., of Chicago, John M. Dallesasse, Univ., of Illinois at Urbana–Champaign, Frederic T. Chong, Univ., of Chicago and Yanjing Li, Univ., of Chicago

[15:40 – 16:00] Coffee Break

[16:00 – 17:15] Special Session 2: Heterogeneous Integration and Interconnect Fabrics

Session Chair: Ishan Thakkar, *Univ., of Kentucky*

Session Organizers: Baris Taskin, *Drexel Univ.,,* Boris Vaisband, *McGill Univ.,*

3D NoCs with Active Interposer for Multi-Chip Module Vasil Pano, Ragh Kuttappa and Baris Taskin, *Drexel Univ.*

Global and Semi-Global Communication on Silicon Interconnect Fabric
Boris Vaisband and Subramanian Iyer, *Univ. of California, Los Angeles*

A 7.5-mW 10-Gb/s 16-QAM Wireline Transceiver with Carrier Synchronization and Threshold Calibration for Mobile Inter-chip Communications in 16-nm FinFET
Jieqiong Du, *Univ. of California, Los Angeles,* Chien-Heng Wong, *Univ. of California, Los Angeles,* Yo-Hao Tu, *National Central Univ.*, Wei-Han Cho, *Univ.,of California, Los Angeles*, Yilei Li, *Univ. of California, Los Angeles*, Yuan Du, *Univ. of California, Los Angeles,* Po-Tsang Huang, *National Chiao Tung Univ.*, Sheau-Jiung Lee, *TSVLink Corp,* and Mau-Chang Frank Chang, *Univ. of California, Los Angeles.*

[17:15 – 17:30] Closing Remarks with Best Paper Announcement

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