CODES+ISSS 2019

Call for Papers

International Conference on Hardware/Software Codesign and System Synthesis
October 13 – October 18, 2019, New York City, USA

The International Conference on Hardware/Software Codesign and System Synthesis is the premier event in system-level design, modeling, analysis, and implementation of modern embedded, IoT, and cyber-physical systems, from system-level specification and optimization down to system synthesis of multi-processor hardware/software implementations. The conference is a forum bringing together academic research and industrial practice for all aspects related to system-level and hardware/software co-design. High-quality original papers will be accepted for oral presentation followed by interactive poster sessions.

Journal track submissions:
Abstract: April 5, 2019
Full paper: April 12, 2019 (firm)
Work in Progress submissions:
June 07, 2019 (firm)
Notification of acceptance
July 10, 2019 (both tracks)

Topics of interest include:

Track 1) System-level design – Specification, modelling, refinement, system synthesis, partitioning, hardware-software co-design, design space exploration, hybrid system modelling and design, model-based design, and design for adaptivity and reconfigurability.

Track 2) Data-driven and application-specific design – Analysis, design, and hardware/software optimization for Big Data and deep learning, and domain-specific hardware/software designs with accelerators, emerging technologies, and approximate computing.

Track 3) Embedded software – Language and library support, compilers, runtimes, parallelization, software verification, memory management, virtual machines, operating systems, real-time support, middleware.

Track 4) Safety, security and reliability – Cross-layer reliability, fault tolerance, design for testability, hardware and software security, security for embedded and IoT devices, and cyber-physical system security.

Track 5) Simulation, validation and verification – Hardware/software co-simulation, verification and validation methodologies, formal verification, hardware accelerated simulation, simulation and verification languages, models, and benchmarks.

Track 6) System architecture – Heterogeneous systems, many-cores, networked and distributed systems, architecture and micro-architecture design, exploration and optimization including application-specific processors, reconfigurable/adaptive architectures, storage, memory and communication systems, and networks-on-chip.

Track 7) Power-aware systems – Power- and energy-aware system design and methodologies ranging from low-power embedded and cyber-physical systems to energy-efficient large-scale systems such as cloud datacenters, supercomputers, green IT, and smart grids.

Track 8) Industrial practices and case studies – Practical impact on current and/or future industries, application of state-of-the-art methodologies and tools in various application areas including wireless, networking, multimedia, automotive, cyber-physical, medical systems, IoT, etc.

A Special Day on the Internet of Medical Things will be organized jointly by all conferences in ESWEEK. Papers aligned to the topics of interest for CODES+ISSS with focus on Cyber-Physical Systems and Networking for Healthcare are welcome.

CODES+ISSS 2019 has a dual publication model where papers will be published in two tracks: Journal track papers will be published in the ACM Transactions on Embedded Computing Systems (TECS) and Work-in-Progress track papers will be published in the ESWEEK Proceedings. More details at http://www.esweek.org/author-information.

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