Embedded Systems Week 2013

September 29th – October 4th, Montréal Marriott Chateau Champlain Hotel, Montreal, Canada

Sep. 29 (SUN)		Room Viger A	Room Viger B	Room Viger C	Room Cartier AB	Room Cartier C
0800-0930		Tutorial 1	Tutorial 2	Tutorial 3	SEC Workshop	WESS Workshop
0930-1000		**Coffee Break (Lower Lobby Ballroom)**				
1000-1200		Tutorial 1	Tutorial 2	Tutorial 3	SEC Workshop	WESS Workshop
1200-1300		**Lunch (Salle de Bal / Foyer)**				
1330-1500		Tutorial 1	Tutorial 4	BES Workshop	SEC Workshop	WESS Workshop
1500-1530		**Coffee Break (Lower Lobby Ball Room)**				
1530-1730		Tutorial 1	Tutorial 4	BES Workshop	SEC Workshop	WESS Workshop
1800-2000		**Welcome Reception (Room TBD)**				
Sep. 30 (MON)	Salle de Bal	Room Cartier C	Room Viger AB	Room Cartier AB	Room Viger C	
0800-0830	Opening Remarks (Plenary)					
0830-0930	Keynote: Clas Jacobson					
0930-1000	**Coffee Break (Lower Lobby Ball Room)**					
1000-1200		CASES Session 1	EMSOFT Session 1	CODES+ISSS Session 1A	CODES+ISSS Session 1B	
1200-1300	**Lunch (Salle de Bal / Foyer)**					
1300-1500		CASES Session 2	EMSOFT Session 2	CODES+ISSS Session 2A	CODES+ISSS Session 2B	
1500-1530	**Coffee Break (Lower Lobby Ball Room)**					
1530-1730		CASES Session 3	EMSOFT Session 3	CODES+ISSS Session 3	Industrial Panel 1	
Oct. 1 (TUE)	Salle de Bal	Room Cartier C	Room Viger AB	Room Cartier AB	Room Viger C	
0830-0930	Keynote: Richard Schooler					
0930-1000	**Coffee Break (Lower Lobby Ball Room)**					
1000-1200		CASES Session 4	EMSOFT Session 4A	CODES+ISSS Session 4	EMSOFT Session 4B	
1200-1300	**Lunch (Salle de Bal / Foyer)**					
1300-1500		CASES Session 5	EMSOFT Session 5A	CODES+ISSS Session 5	EMSOFT Session 5B	
1500-1530	**Coffee Break (Lower Lobby Ball Room)**					
1530-1730		CASES Session 6	EMSOFT Session 6	CODES+ISSS Session 6	Industrial Panel 2	
1830-2030	**Banquet Gala (Room TBD)**					
Oct. 2 (WED)	Salle de Bal	Room Cartier C	Room Viger AB	Room Cartier AB	Room Viger C	
0830-0930	Keynote: Michel Laurence					
0930-1000	**Coffee Break (Lower Lobby Ball Room)**					
1000-1200		CASES Session 7	EMSOFT Session 7	CODES+ISSS Session 7A	CODES+ISSS Session 7B	
1200-1300	**Lunch (Salle de Bal / Foyer)**					
1300-1500		CASES Session 8	EMSOFT Session 8	CODES+ISSS Session 8A	CODES+ISSS Session 8B	
1500-1530	**Coffee Break (Lower Lobby Ball Room)**					
1530-1730	Panel (Plenary Session)					
1730-1745	Best Paper Awards, Closing Remarks (Plenary)					
Oct. 3 (THU)	Room Cartier A	Room Cartier B	Room Cartier C	Room Viger B	Room Viger C	Room CafConc
0800-0930	ESTIMedia	RSP	MeAOW	CASA	WESE	MCES
0930-1000	**Coffee Break (Lower Lobby Ball Room)**					
1000-1200	ESTIMedia	RSP	MeAOW	CASA	WESE	MCES
1200-1300	**Lunch (Salle de Bal / Foyer)**					
1300-1500	ESTIMedia	RSP	MeAOW	CASA	WESE	MCES
1500-1530	**Coffee Break (Lower Lobby Ball Room)**					
1530-1730	ESTIMedia	RSP	MeAOW	CASA	WESE	MCES
Oct. 4 (FRI)	Room Maisonneuve A	Maisonneuve D	Maisonneuve E	Maisonneuve F		
0800-0930	ESTIMedia	RSP	WSS	EON		
0930-1000	**Coffee Break (Room TBD)**					
1000-1200	ESTIMedia	RSP	WSS	EON		

MONDAY, SEPTEMBER 30th

CASES	CODES+ISSS	EMSOFT
Opening Remarks		
Keynote Speech #1		
Session 1: Reconfigurable Computing **1.1 Aging-aware Hardware-Software Task Partitioning for Reliable Reconfigurable Multiprocessor Systems** *Anup Das, Akash Kumar and Bharadwaj Veeravalli* **1.2 Scrubbing Unit Repositioning for Fast Error Repair in FPGAs** *Gabriel Nazar, Leonardo Santos and Luigi Carro* **1.3 Compiled Multithreaded Data Paths on FPGAs for Dynamic Workloads** *Robert Joseph Halstead and Walid Najjar*	**Session 1A: Various Facets of Memory Optimization** **★ 1A.1 Reducing Inter-Core Cache Contention with an Adaptive Bank Mapping Policy in DRAM Cache** *Fazal Hameed, Lars Bauer and Jorg Henkel* **1A.2 A Reconfigurable Real-Time SDRAM Controller for Mixed Time-Criticality Systems** *Sven Goossens, Jasper Kuijsten, Benny Akesson and Kees Goossens* **1A.3 A DRAM-Flash Index for Native Flash File Systems** *Chien-Chung Ho, Po-Chun Huang, Yuan-Hao Chang and Tei-Wei Kuo* **Session 1B: Novel Alternative Embedded System Architectures** **1B.1 WHISK: An Uncore Architecture for Dynamic Information Flow Tracking in Heterogeneous Processors** *Joel Porquet and Simha Sethumadhavan* **1B.2 Synthesis-friendly Techniques for Tightly-coupled Integration of Hardware Accelerators into Shared-memory Multi-core Clusters** *Francesco Conti, Andrea Marongiu and Luca Benini* **1B.3 Embedded Supercomputing in FPGAs with the MXP Matrix Processor** *Aaron Severance and Guy Lemieux*	**Session 1: Programming Languages and Models of Computation** **★1.1 A Synchronous Embedding of Antescofo, a Domain-Specific Language for Interactive Mixed Music** *Guillaume Baudart, Florent Jacquemard, Louis Mandel and Marc Pouzet* **1.2 Determinate Composition of FMUs for Co-Simulation** *David Broman, Christopher Brooks, Lev Greenberg, Edward A. Lee, Stavros Tripakis, Michael Wetter and Michael Masin* **1.3 BPDF: A Statically Analyzable DataFlow Model with Integer and Boolean parameters** *Vagelis Bebelis, Pascal Fradet, Alain Girault and Bruno Lavigueur*
Session 2: Specifying and Exploiting Parallelism **2.1 Automatic Extraction of Pipeline Parallelism for Embedded Heterogeneous Multi-Core Platforms** *Daniel Cordes, Michael Engel, Olaf Neugebauer and Peter Marwedel* **★ 2.2 Expandable Process Networks to Efficiently Specify and Explore Task, Data, and Pipeline Parallelism** *Lars Schor, Hoeseok Yang, Iuliana Bacivarov and Lothar Thiele* **2.3 A Novel Compilation Approach for Image Processing Graphs on a Many-Core Platform with Explicitly Managed Memory** *Thierry Lepley, Pierre Paulin and Eric Flamand*	**Session 2A: Power and Energy Aware Systems** **2A.1 DHeating: Dispersed Heating Repair for Self-Healing NAND Flash Memory** *Renhai Chen, Yi Wang and Zili Shao* **2A.2 Learning the Optimal Operating Point for Many-Core Systems with Extended Range Voltage/Frequency Scaling** *Da-Cheng Juan, Siddharth Garg, Jinpyo Park and Diana Marculescu* **2A.3 Online OLED Dynamic Voltage Scaling for Video Streaming Applications on Mobile Devices** *Mengying Zhao, Hao Zhang, Xiang Chen, Yiran Chen and Chun Jason Xue* **Session 2B: Managing Accelerators in Heterogeneous Platforms** **2B.1 pvFPGA: Accessing an FPGA-based Hardware Accelerator in a Paravirtualized Environment** *Miodrag Bolic, Wei Wang and Jonathan Parri* **2B.2 An Efficient and Effective Code Management for Software Managed Multicores** *Jing Lu, Ke Bai and Aviral Shrivastava* **2B.3 On the Automatic Generation of GPU-oriented Software Applications from RTL IPs** *Nicola Bombieri, Franco Fummi and Sara Vinco*	**Session 2: Systems** **2.1 An Efficient Code Update Solution for Wireless Sensor Network Reprogramming** *Biswajit Mazumder and Jason O. Hallstrom* **2.2 Middleware Design for Physically-Asynchronous Logically-Synchronous (PALS) Systems** *Abdullah Al-Nayeem, Cheolgi Kim, Woochul Kang, Po-Liang Wu and Lui Sha* **2.3 Diversifying Wear Index for MLC NAND Flash Memory to Extend the Lifetime of SSDs** *Yeong-Jae Woo and Jin-Soo Kim*
Session 3: Compilers **3.1 Exploiting Phase Inter-Dependencies for Faster Iterative Compiler Optimization Phase Order Searches** *Michael Jantz and Prasad Kulkarni* **3.2 Platform-Dependent Code Generation for Embedded Real-Time Software** *BaekGyu Kim, Linh T.X. Phan, Insup Lee and Oleg Sokolsky* **3.3 CAeSaR: Unified Cluster-Assignment Scheduling and Communication Reuse for Clustered VLIW Processors** *Vasileios Porpodas and Marcelo Cintra*	**Session 3: Special Session - Run-Time Adaption for Highly-Complex Multi-Core Systems** **3.1 The Thermal Problem: Scalable Adaptive Solutions for Complex Multi-core Systems** *Jörg Henkel* **3.2 Flexing Adaptive Voltage Scaling using Hybrid CMOS-Steep Slope Transistor Technology** *Vijaykrishnan Narayanan* **3.3 Highly Adaptive Pipelined Architectures for Complex Multi-Media Applications** *Sri Parameswaran* **3.4 The Invasive Computing Paradigm as a Solution for Highly Adaptive and Efficient Multi-core Systems** *Jürgen Teich*	**Session 3: Verification I** **★3.1 Safety Verification for Linear Systems** *Sridhar Duggirala and Ashish Tiwari* **3.2 Bit-precise Formal Verification of Discrete-Time MATLAB/Simulink Models using SMT Solving** *Paula Herber, Robert Reicherdt and Patrick Bittner* **3.3 Verifying Simulink Diagrams Via A Hybrid Hoare Logic Prover** *Liang Zou, Naijun Zhan, Shuling Wang, Martin Fränzle and Shengchao Qin*

★ denotes candidate best paper.

TUESDAY, OCTOBER 1st

CASES	CODES+ISSS	EMSOFT
Keynote speech #2		
Session 4: Memory Systems **4.1 Hybrid Compile and Run-Time Memory Management for a 3D-Stacked Reconfigurable Accelerator** *Lovic Gauthier, Shinya Ueno and Koji Inoue* **4.2 Simultaneously Optimizing DRAM Cache Hit Latency and Miss Rate via Novel Set Mapping Policies** *Fazal Hameed, Lars Bauer and Jörg Henkel* **4.3 Minimizing Code Size via Page Selection Optimization on Partitioned Memory Architectures** *Yuan Mengting, Chun Jason Xue, Chen Yong, Qingan Li and Yingchao Zhao*	**Session 4: System- and High-level Synthesis** **4.1 Bound-Oriented Parallel Pruning Approaches for Efficient Resource Constrained Scheduling of High-Level Synthesis** *Mingsong Chen, Lei Zhou, Geguang Pu and Jifeng He* **★ 4.2 Improving Polyhedral Code Generation for High-Level Synthesis** *Wei Zuo, Peng Li, Deming Chen, Louis-Noel Pouchet, Shunan Zhong and Jason Cong* **4.3 System Level Synthesis of Hardware for DSP Applications Using Pre-Characterized Function Implementations** *Shuo Li, Nasim Farahini, Ahmed Hemani, Kathrin Rosvall and Ingo Sander*	**Session 4A: System-Level Modeling and Analysis** **4A.1 A Characterization of Integrated Multi-View Modeling for Embedded Systems** *Magnus Persson, Martin Törngren, Ahsan Qamar, Jonas Westman, Matthias Biehl, Stavros Tripakis, Hans Vangheluwe and Joachim Denil* **4A.2 Diversely Enumerating System-Level Architectures** *Ethan K. Jackson, Gabor Simko and Janos Sztipanovits* **4A.3 On the Schedulability of Real-Time Discrete-Event Systems** *Eleftherios Matsikoudis, Christos Stergiou and Edward Lee* **Session 4B: Verification II** **4B.1 On Composing and Proving the Correctness of Reactive Behavior** *David Harel, Amir Kantor, Guy Katz, Assaf Marron, Lior Mizrahi and Gera Weiss* **4B.2 Time-aware Relational Abstractions for Hybrid Systems** *Sergio Mover, Alessandro Cimatti, Ashish Tiwari and Stefano Tonetta* **4B.3 Path-Sensitive Resource Analysis Compliant with Assertions** *Duc-Hiep Chu and Joxan Jaffar*
Session 5: Heterogeneous Architectures **★ 5.1 EVA: An Efficient Vision Architecture for Mobile Systems** *Jason Clemons, Andrea Pellegrini, Silvio Savarese and Todd Austin* **5.2 Hardware Acceleration for Programs in SSA Form** *Manuel Mohr, Artjom Grudnitsky, Tobias Modschiedler, Lars Bauer, Sebastian Hack and Jörg Henkel* **5.3 Power-Performance Modeling on Asymmetric Multi-Cores** *Mihai Pricopi, Thannirmalai Somu Muthukaruppan, Vanchinathan Venkataramani, Tulika Mitra and Sanjay Vishin*	**Session 5: Medical and Bio-inspired Embedded Systems** **5.1 A Cyber-Physical System Approach to Artificial Pancreas Design** *Mahboobeh Ghorbani and Paul Bogdan* **5.2 Accelerating Floating Point Time-Series Subsequences using Instruction Set Extensions for Embedded Systems** *Joseph Tarango, Philip Brisk and Eamonn Keogh* **5.3 Scalable NoC-Based Architecture of Neural Coding for New Efficient Associative Memories** *Jean-Philippe Diguet, Martha Johanna Sepulveda, Nicolas Le Griguer, Lydie Caetano and Marius Strum*	**Session 5A: Scheduling and Timing Analysis** **5A.1 Simple Analysis of Partial Worst-case Execution Paths on General Control Flow Graphs** *Jan Kleinsorge, Heiko Falk and Peter Marwedel* **5A.2 Scheduling of Mixed-Criticality Applications on Resource-Sharing Multicore Systems** *Georgia Giannopoulou, Nikolay Stoimenov, Pengcheng Huang and Lothar Thiele* **5A.3 Limited Preemptive Scheduling of Non-independent Task Sets** *Andrea Baldovin, Enrico Mezzetti and Tullio Vardanega* **Session 5B: Special Session - Safety critical and Mixed Critical Systems Research - Are we Addressing the Right Challenges?** *Speakers: TBA*
Session 6: Special Session - Sustaining Moore's Law: Specialization to the Rescue **6.1 Bitcoin and The Age of Bespoke Silicon**, *Michael B. Taylor* **6.2 Dynamic Hardware Specialization - Using Moore's Bounty Without Burning the Chip Down** *Karu Sankaralingam* **6.3 From Software to Accelerators with LegUp High-Level Synthesis** *Andrew Canis, Jongsok Choi, Blair Fort, Ruolong Lian, Qijing Huang, Nazanin Calagard, Marcel Gort, Jia Jun Qin, Mark Aldham, Tomasz Czajkowski, Stephen Brown and Jason Anderson* **6.4 Toward Affordable Customization** *Todd Austin*	**Session 6: Special Session - Silicon Brain - Emerging Neuromorphic Computing Architecture and Systems** **6.1 Design Space Exploration and Parameter Tuning for Neuromorphic Applications** *Jeff Krichmar* **6.2 Unconventional Energy-Efficient and Fault-Tolerant Accelerators** *Olivier Temam* **6.3 Embedded Neuromorphic Vision Systems** *Kevin Irick* **6.4 Bio-Inspired Ultra Lower-Power Neuromorphic Computing Engine for Embedded Systems** *Yiran Chen*	**Session 6: Performance Management and Resource Awareness** **6.1 A Generalized Software System for Accurate and Efficient Management of Application Performance Goals** *Henry Hoffmann, Martina Maggio, Marco D. Santambrogio, Alberto Leva and Anant Agarwal* **6.2 StreaMorph: A Case for Synthesizing Energy-Efficient Adaptive Programs Using High-Level Abstractions** *Dai Bui and Edward Lee* **6.3 Energy-Efficient Thread Co-Scheduling in Heterogeneous Multicore Processors** *Rajiv Nishtala, Daniel Mossé and Vinicius Petrucci*

WEDNESDAY, OCTOBER 2nd

CASES	CODES+ISSS	EMSOFT
Keynote speech #3		
Session 7: Analysis and Tools **7.1 Effective Code Discovery for ARM/Thumb-1 Mixed ISA Binaries in a Static Binary Translator** *Jiunn-Yeu Chen, Bor-Yeh Shen, Quan-Huei Ou, Wuu Yang and Wei-Chung Hsu* **★7.2 ILPc: A Novel Approach for Scalable Timing Analysis of Synchronous Programs** *Jia Jie Wang, Partha Roop and Sidharta Andalam* **7.3 SPM-Sieve: A Framework for Assisting Data Partitioning in Scratch Pad Memory Based Systems** *Prasenjit Chakraborty and Preeti Ranjan Panda*	**Session 7A: Design Techniques for Automotive Systems** **7A.1 IVaM: Implicit Variant Modeling and Management for Automotive Embedded Systems** *Sebastian Graf, Michael Glaß, Dominic Wintermann, Jürgen Teich and Christoph Lauer* **7A.2 Improved Formal Worst-Case Timing Analysis of Weighted Round Robin Scheduling for Ethernet** *Daniel Thiele, Jonas Diemer, Philip Axer, Rolf Ernst and Jan Seyler* **★ 7A.3 Dimensioning and Configuration of EES Systems for Electric Vehicles with Boundary-Conditioned Adaptive Scalarization** *Wanli Chang, Martin Lukasiewycz, Sebastian Steinhorst and Samarjit Chakraborty* **Session 7B: Efficient Emulation and Validation Techniques** **7B.1 VarEMU: An Emulation Testbed for Variability-Aware Software** *Lucas Wanner, Salma Elmalaki, Liangzhen Lai, Puneet Gupta and Mani Srivastava* **7B.2 Automatic Generation of Compact Formal Properties for Effective Error Detection** *Michele Bertasi, Giuseppe Di Guglielmo and Graziano Pravadelli* **7B.3 Automatic Refinement of Requirements for Verification throughout the SoC Design Flow** *Laurence Pierre and Zeineb Bel Hadj Amor*	**Session 7: Embedded Control and Synthesis** **7.1 Synthesis of Fixed-Point Programs** *Eva Darulova, Viktor Kuncak, Rupak Majumdar and Indranil Saha* **7.2 Stability-Aware Analysis and Design of Embedded Control Systems** *Amir Aminifar, Petru Eles, Zebo Peng and Anton Cervin* **7.3 Pre-orders for Reasoning about Stability Properties with respect to Inputs of Hybrid Systems** *Pavithra Prabhakar, Jun Liu and Richard M. Murray*

Session 8: Fault Tolerance and Security **8.1 Fault Detection and Recovery Efficiency Co-optimization Through Compile-time Analysis and Runtime Adaptation** *Hao Chen and Chengmo Yang* **8.2 Global Property Violation Detection and Diagnosis for Wireless Sensor Networks** *Man Wang and Zhiyuan Li* **8.3 An Efficient Run-time Encryption Scheme for Non-volatile Main Memory** *Xian Zhang, Chao Zhang, Guangyu Sun, Tao Zhang and Jia Di*	**Session 8A: Large Scale and Emerging Architectures** **8A.1 ARGO: Aging-awaRe GPGPU Register File AllOcation** *Majid Namaki-Shoushtari, Abbas Rahimi, Nikil Dutt, Puneet Gupta and Rajesh Gupta* **8A.2 An Energy and Deadline Aware Resource Provisioning, Scheduling and Optimization Framework for Cloud Systems** *Yue Gao, Yanzhi Wang, Sandeep Gupta and Massoud Pedram* **8A.3 Designing a Residential Hybrid Electrical Energy Storage System Based on the Energy Buffering Strategy** *Di Zhu, Siyu Yue, Yanzhi Wang, Younghyun Kim, Naehyuck Chang and Massoud Pedram* **Session 8B : Evaluation of Timing & Energy Metrics in Embedded Software** **8B.1 Panappticon: Event-based Tracing to Optimize Mobile Application and Platform Performance** *Lide Zhang, David R. Bild, Robert P. Dick, Z. Morley Mao and Peter Dinda* **8B.2 Multi-Mode Monitoring for Mixed-Criticality Real-time Systems** *Moritz Neukirchner, Kai Lampka, Sophie Quinton and Rolf Ernst* **8B.3 A Variability-Aware OpenMP Environment for Efficient Execution of Accuracy-Configurable Computation on Shared-FPU Processor Clusters** *Abbas Rahimi, Andrea Marongiu, Rajesh K. Gupta and Luca Benini* **8B.4 Automated, Retargetable Back-Annotation for Host Compiled Performance and Power Modeling** *Suhas Chakravarty, Zhuoran Zhao and Andreas Gerstlauer*	**Session 8: Dynamic Analysis** **8.1 DIME: Time-aware Dynamic Binary Instrumentation Using Rate-based Resource Allocation** *Pansy Arafa, Hany Kashif and Sebastian Fischmeister* **8.2 Verification of Annotated Models from Executions** *Parasara Sridhar Duggirala, Sayan Mitra and Mahesh Viswanathan* **8.3 WakeScope: Runtime WakeLock Anomaly Management Scheme for Android Platform** *Kwanghwan Kim and Hojung Cha*
Closing Session (Plenary): ESWEEK – Looking at Past Data to Improve the Future (PANEL) *Organizer: Reinaldo A. Bergamaschi; Moderators: Reinaldo A. Bergamaschi and Donald Thomas* *Speakers: Petru Eles, Soonhoi Ha, Ahmed Jerraya, Christoph Kirsch, Pierre Paulin, and Marilyn Wolf* Followed by announcement of best paper awards and closing remarks		

SYMPOSIA, WORKSHOPS AND TUTORIALS

SUNDAY, SEPTEMBER 29th: TUTORIALS

Tutorial 1: Methodologies and Tools for Embedded Multisensory Systems Based on ARM Cortex-M Processors *Organizer and Speaker: Zeljko Zilic, (McGill)*	**Tutorial 2: AADLv2, an Architecture Description Language for the Analysis and Generation of Embedded Systems** *Organizers and Speakers: Jerome Hugues (ISAE/DMIA) and Frank Singhoff (UBO/Lab-STICC)* **Tutorial 4: Mixed-criticality Systems: Design and Certification Challenges** *Organizers: Madeleine Faugere (Thales), Nikolay Stoimenov (ETH Zurich) and Lothar Thiele (ETH Zurich)* *Speakers: Madeleine Faugere (Thales Research and Technology), James Anderson (University of North Carolina at Chapel Hill), Claire Pagetti (Onera), Pierre Bieber (Onera), Virginie Wiels (Onera) and Marc Gatti (Thales Avionics)*	**Tutorial 3: Cross-Layer Reliability Modeling and Optimization for Embedded Systems under Process Variations** *Organizers and Speakers: Muhammad Shafique (Karlsruhe Institute of Technology), Puneet Gupta (UCLA), Hiren Patel (Univ. of Waterloo) and Siddharth Garg (Univ. of Waterloo)*

SUNDAY, SEPTEMBER 29th: WORKSHOPS

BES 2013: Benchmarking of Embedded Systems Workshop *Organizers: Sebastian Fischmeister (Univ. of Waterloo), Peter Stokes (CMC Microsystems), Shay Gal-On (EEMBC) and Darshika Perera (CMC Microsystems)*

SEC 2013: First International Workshop on the Swarm at the Edge of the Cloud *Organizers: Jan Rabaey (UC Berkeley), Prabal Dutta (Univ. of Michigan) and George Pappas (Univ. of Pennsylvania)*

WESS 2013: Workshop on Embedded Systems Security *Organizers: Catherine Gebotys (Univ. of Waterloo), Dimitrios Serpanos (Univ. of Patras) and Marilyn Wolf (Georgia Tech)*

MONDAY, SEPTEMBER 30th: INDUSTRY PANEL

Industry Panel 1: System-Level Design and High-Level Synthesis *Organizer and Moderator: Andreas Gerstlauer (Univ of Texas); Speakers: Yatin Hoskote (Intel), Rishiyur Nikhil (Bluespec), John Sanguinetti (Forte) and Andres Takach (Calypto).*

TUESDAY, OCTOBER 1st: INDUSTRY PANEL

Industry Panel 2: Modeling Complex Industrial Systems *Organizer and Moderator: Alessandro Pinto (UTRC); Speakers: Alberto Ferrari (Ales), Pieter Mosterman (The Mathworks) and Claudio Pinello (UTRC).*

THURSDAY, OCTOBER 3rd: SYMPOSIA AND WORKSHOPS

ESTIMedia 2013: Symposium on Embedded Systems for Real-Time Multimedia *Organizers: Jian-Jia Chen (KIT), Maurizio Palesi (Kore Univ.), Todor Stefanov (Leiden Univ.)*

RSP 2013: IEEE International Symposium on Rapid System Prototyping *Organizers: Fabiano Hessel (PUCS), Jérôme Hugues (ISAE), Frédéric Rousseau (TIMA)*

CASA 2013: Workshop on Compiler Assisted SoC Assembly *Organizers: Brett Meyer (McGill Univ.)*

MeAOW 2013: Memory Architecture and Organization Workshop *Organizers: Nikil Dutt (Univ. of California at Irvine), and Chun Jason Xue (City Univ. of Hong Kong)*

MCES 2013: Workshop on Many-Core Embedded Systems *Organizers: Yassine Hariri (CMC Microsystems), and Pierre Paulin (STMicroelectronics)*

WESE 2013: Workshop on Embedded and Cyber-Physical Systems Education *Organizers: Peter Marwedel (TU Dortmund), Kenneth Ricks (Univ. of Alabama), and Jeff Jackson (Univ. of Alabama)*

FRIDAY, OCTOBER 4th: SYMPOSIA AND WORKSHOPS

ESTIMedia 2013: Symposium on Embedded Systems for Real-Time Multimedia *Organizers: Jian-Jia Chen (KIT), Maurizio Palesi (Kore Univ.), Todor Stefanov (Leiden Univ.)*

RSP 2013: IEEE International Symposium on Rapid System Prototyping *Organizers: Fabiano Hessel (PUCS), Jérôme Hugues (ISAE), Frédéric Rousseau (TIMA)*

EON 2013: Workshop on Optimization of Computing at the Edge of the Network *Organizers: Shahrokh Daijavad (IBM) and Seraphin Calo (IBM)*

WSS 2013: Workshop on Software Synthesis *Organizers: Peter Marwedel (TU Dortmund), and Alberto Sangiovanni-Vincentelli (UC Berkeley)*