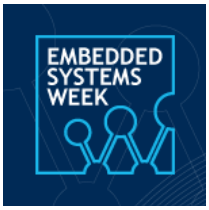

Embedded Systems Week 2014

October 12th – 17th, Jaypee Greens, New Delhi, India

Oct 12 (Sun)	Maple	Oak	Cedar	Royal Ballroom 1	Royal Ballroom 2
0800-0930	Tutorial 1	Tutorial 2	Tutorial 4	ARM Training Workshop	Tutorial 5
0930-1000	Coffee Break				
1000-1200	Tutorial 1	Tutorial 2	Tutorial 4	ARM Training Workshop	Tutorial 5
1200-1300	Lunch				
1300-1500	Xilinx Workshop	Tutorial 2	Tutorial 3	ARM Training Workshop	Tutorial 5
1500-1530	Coffee Break				
1530-1700	Xilinx Workshop	Tutorial 2	Tutorial 3	ARM Training Workshop	Tutorial 5
1800-2000	Welcome Reception				
Oct 13 (Mon)	**Maple**	**Oak**	**Cedar**	**Royal Ballroom 1**	
0800-0830	Opening Session				
0830-0930	Keynote: “System of Systems and Geography of Computing”, Jaswinder S. Ahuja, Cadence				
0930-1000	Coffee Break				
1000-1200	CODES+ISSS Session 1B	EMSOFT Session 1	CASES Session 1	CODES+ISSS Session 1A	
1200-1300	Lunch				
1300-1500	CODES+ISSS Session 2B	EMSOFT Session 2	CASES Session 2	CODES+ISSS Session 2A	
1500-1530	Coffee Break				
1530-1730	CODES+ISSS Session 3	EMSOFT Session 3	CASES Session 3A	CASES Session 3B	
1800-1845	Cultural Program				
Oct 14 (Tue)	**Maple**	**Oak**	**Cedar**	**Royal Ballroom 1**	
0830-0930	Keynote: “Emerging Trends in Electronics in an Intelligent Connected World”, Guru Ganesan, ARM				
0930-1000	Coffee Break				
1000-1200	EMSOFT Session 4A	EMSOFT Session 4B	CASES Session 4	CODES+ISSS Session 4	
1200-1300	Lunch				
1300-1500	EMSOFT Session 5A	EMSOFT Session 5B	CASES Session 5	CODES+ISSS Session 5	
1500-1530	Coffee Break				
1530-1730	EMSOFT Session 6A	EMSOFT Session 6B	CASES Session 6	CODES+ISSS Session 6	
1800-2100	Reception, Keynote: “Simulation is Passé; all Future Systems Require FPGA Prototyping”, Prof. Arvind, MIT, and Banquet				
Oct 15 (Wed)	**Maple**	**Oak**	**Cedar**	**Royal Ballroom 1**	
0830-0930	Keynote: “Smart energy: Ubiquitous Role of Embedded Systems”, Prof. Krithi Ramamritham, IITB				
0930-1000	Coffee Break				
1000-1200	CODES+ISSS Session 7A	EMSOFT Session 7	CASES Session 7	CODES+ISSS Session 7B	
1200-1300	Lunch				
1300-1500	CODES+ISSS Session 8A	EMSOFT Session 8	CASES Session 8	CODES+ISSS Session 8B	
1500-1530	Coffee Break				
1530-1730	Panel: ESWEEK at Crossroads: New Applications, New Challenges, and the Road Ahead Toward Designing New "Things"				
1730-1745	Closing and Best Paper Awards				
Oct 16 (Thu)	**Maple**	**Oak**	**Cedar**	**Meeting Room 1**	**Meeting Room 2**
0800-0930	RSP	ESTIMedia	MeAOW	WESE	CASA
0930-1000	Coffee Break				
1000-1200	RSP	ESTIMedia	MeAOW	WESE	CASA
1200-1300	Lunch				
1300-1500	RSP	ESTIMedia	MeAOW	WESE	CASA
1500-1530	Coffee Break				
1530-1730	RSP	ESTIMedia	MeAOW	WESE	CASA
Oct 17 (Fri)	**Maple**	**Oak**	**Cedar**	**Meeting Room 1**	**Meeting Room 2**
0800-0930	RSP	ESTIMedia	IPEDV	CPSArch	WESS
0930-1000	Coffee Break				
1000-1200	RSP	ESTIMedia	IPEDV	CPSArch	WESS
1200-1300	Lunch				
1300-1500			IPEDV	CPSArch	WESS
1500-1530	Coffee Break				
1530-1730			IPEDV	CPSArch	WESS

Sunday	Tutorials	Tutorials	Tutorials	Tutorials	Training Workshop
8.00 – 9.30	Tutorial 1: Formal Verification of Simulink/Stateflow Diagrams	Tutorial 2: Run-time Reconfigurable High Performance SoCs	Tutorial 4: Mitigation of soft errors: from adding selective redundancy to changing the abstraction stack	Tutorial 5: Modeling, Validation and Synthesis of Embedded Control Software	ARM Training Workshop
9.30 – 10.00	Coffee Break				
10.00 – 12.00	Tutorial 1: Formal Verification of Simulink/Stateflow Diagrams	Tutorial 2: Run-time Reconfigurable High Performance SoCs	Tutorial 4: Mitigation of soft errors: from adding selective redundancy to changing the abstraction stack	Tutorial 5: Modeling, Validation and Synthesis of Embedded Control Software	ARM Training Workshop
12.00 – 13.00	Lunch				
13.00 – 15.00	Xilinx Workshop	Tutorial 2: Run-time Reconfigurable High Performance SoCs	Tutorial 3: Methods and tools for smart device integration and simulation	Tutorial 5: Modeling, Validation and Synthesis of Embedded Control Software	ARM Training Workshop
15.00 – 15.30	Coffee Break				
15.30 – 17.00	Xilinx Workshop	Tutorial 2: Run-time Reconfigurable High Performance SoCs	Tutorial 3: Methods and tools for smart device integration and simulation	Tutorial 5: Modeling, Validation and Synthesis of Embedded Control Software	ARM Training Workshop
18.00-20.00	**Welcome Reception**				

Plenary Keynotes

8.30 am, Monday, October 13th

System of Systems and the Geography of Computing

Jaswinder S. Ahuja
Corporate Vice President and Managing Director, Cadence Design Systems

Abstract
System of systems is a collection of systems that pool their resources and capabilities together to create a new, more complex system which offers more functionality and performance than simply the sum of the constituent systems. For example, a car is a complex system made up of over 40 electronic systems for airbag deployment, cruise control, entertainment, braking, etc. Similar examples are all around us – from mobile devices to gaming consoles to home electronics. In the Internet of Things (IOT) era, all these systems are interconnected either to the home, to the city or to the cloud. This connectivity brings system-level challenges include partitioning, communications protocols, IP selection, software bring-up, hardware-software verification, reliability, safety, and more. The electronic systems that make up the IOT generate huge amounts of data, and data is useful only when we compute on it and share it. When the dimensions of design range from few nm to thousands of kilometers, geography of computing is key. This presentation talks about innovation in system of systems, its context in the Internet of Things era, and the geography of computing in terms of data and energy.

Biography
Jaswinder S. Ahuja is a Corporate Vice President and the Managing Director of Cadence Design Systems in India. Jaswinder heads Cadence's India Field Operations and the India Operating Region. He is also responsible for Global Customer Support and Education Services. Jaswinder is a founding member and the current President of the VLSI Society of India (VSI) and is on the Executive Council of the Indian Electronics & Semiconductor Association (IESA). He served as IESA Chairman in 2007-08. Jaswinder has a B.Tech in Electronics Engineering from IT-BHU, Varanasi and an MS in Computer Engineering from Northeastern University, Boston, USA. He also holds an Executive MBA from Stanford University, USA.

8.30 am, Tuesday, October 14th

Emerging Trends in Electronics in an Intelligent Connected World

Guru Ganesan
President and Managing Director, ARM India

Abstract
With nearly eight Billion people on our planet, it is more imperative now than ever before for each one of us to be able to manage our lives efficiently amidst competing resources, time crunches and the unintentional intrusions in our lives. At the same time, serendipitously, low-power embedded technology has matured to a level where it can be used to bring about the kind of connectivity required of ourselves with everything around us to enable us to overcome the challenges imposed on us by our benevolent, yet overcrowded, planet. The presentation elucidates how the challenges thrown up by the need for this connectivity together with mobility are being addressed in both hardware and software. Furthermore, to the discerning listener, it will become amply clear that our quest for constant connectivity not only carries with it the glam of the possibility of embarking on new areas of growth and research, but also the potential to burden us with a gazillion or more of pieces of information and consequently the responsibility to handle this information efficiently and with appropriate care.

Biography

Guru Ganesan started his career with Tata Consultancy Services. He then had stints at Hewlett-Packard in Cupertino, Cadence Design Systems in San Jose and Texas Instruments in Dallas. Later, in Jan 2001, he was the Director of Engineering in a business unit of Synopsys in Mountain View that got acquired by Artisan Components. In 2002, Mr. Ganesan relocated to India to set up the India operations of Artisan. He was Managing Director of Artisan in India until 2004, when Artisan got acquired by ARM, the world leader in Semiconductor IP. At ARM, Guru has held a variety of positions, starting with Vice President of Engineering in San Jose. He became the Managing Director of ARM India in 2009 and is now its President.

6.30 pm, Tuesday, October 14th

Simulation is Passé; all Future Systems Require FPGA Prototyping

Arvind

Johnson Professor of Computer Science and Engineering, Massachusetts Institute of Technology

Abstract

Power and energy dominate the design of all systems today from smart phones to Internet-of-Things to gigantic data centers. The single most promising approach to reducing power is replacing compute intensive software by special purpose hardware. Without hardware specialization, a smart phone wouldn't have so many different radios or high-resolution cameras or high quality audio or video or GPS navigation. Whether this capability is delivered via ASICs or reconfigurable logic, the designers of such systems have to be proficient in both hardware and software to understand the trade-offs. Large FPGAs with modern high-level hardware synthesis tools offer a design flow that is essential to mitigate development risks without increasing the time-to-market. We will illustrate the power of this design flow via numerous working prototypes developed by us.

Biography

Arvind is the Johnson Professor of Computer Science and Engineering at MIT. Arvind's group, in collaboration with Motorola, built the Monsoon dataflow machines and its associated software in the late eighties. In 2000, Arvind started Sandburst which was sold to Broadcom in 2006. In 2003, Arvind co-founded Bluespec Inc., an EDA company to produce a set of tools for high-level synthesis. In 2001, Dr. R. S. Nikhil and Arvind published the book "Implicit parallel programming in pH". Arvind's current research focus is on enabling rapid development of embedded systems. Arvind is a Fellow of IEEE and ACM, and a member of the National Academy of Engineering and the American Academy of Arts and Sciences.

8.30 am, Wednesday, October 15th

Smart Energy: Ubiquitous Role of Embedded Systems

Krithi Ramamritham

Vijay and Sita Vashee Chair Professor, Indian Institute of Technology Bombay

Abstract

Smart grids have been heralded as the key enabler of cleaner, cheaper and more reliable energy. They incorporate diverse energy sources, advanced monitoring, demand-side management and the ability to "self heal". The success of smart grids lies in the development of effective solutions for a) Demand-supply management incorporating intermittent, renewable, energy sources; b) Monitoring and sensing to understand energy generation and consumption patterns; and c) Distributed information management and control strategies. The talk will cover these topics and show how Embedded Systems play a crucial role in addressing these problems.

Biography

After his B.Tech (Electrical Engineering) and M.Tech (Computer Science) degrees from IIT Madras, Prof. Krithi Ramamritham went on to receive his Ph.D. in Computer Science from the University of Utah. After a long stint at the University of Massachusetts, he moved to IIT Bombay as the Vijay and Sita Vashee Chair Professor in the Department of Computer Science and Engineering. During 2006-2009, he served as Dean (R&D) at IIT Bombay.

Prof. Ramamritham's research explores timeliness and consistency issues in computer systems, in particular, databases, real-time systems, and distributed applications. His recent work addresses these issues in the context of sensor networks, embedded systems, mobile environments and smart grids. During the last few years he has been interested in the use of Information and Communication Technologies for creating tools aimed at socio-economic development.

Prof. Ramamritham is a Fellow of the IEEE, ACM, Indian Academy of Sciences, National Academy of Sciences, India, and the Indian National Academy of Engineering. Twice he has received the IBM Faculty Award. He is also a recipient of the Distinguished Alumnus Award from IIT Madras and the Doctor of Science (Honoris Causa) from the University of Sydney.

Prof. Ramamritham has been associated with the editorial board of various journals. These include IEEE Embedded Systems Letters and Springer's Real-Time Systems Journal (Editor-in-Chief), IEEE Transactions on Knowledge and Data Engineering, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Mobile Computing, IEEE Internet Computing and the VLDB (Very Large Databases) Journal. Moreover, he has served on the Board of Directors of Persistent Systems, Pune, on the Board of Trustees of the VLDB Endowment, and on the Technical Advisory Board of TTTech, Vienna, Austria, Microsoft Research India, and Tata Consultancy Services.

Of the two startups that he has co-founded, Agrocom offers award-winning information and communication technology-based real-time decision-support tools to farmers and organizations enabling progressive farming while Nex Robotics delivers high quality products in robotics and embedded systems.

Plenary Panel

3.30 pm, Wednesday, October 15th

ESWEEK at Crossroads: New Applications, New Challenges, and the Road Ahead Toward Designing New "Things"

Organizer: Radu Marculescu (Carnegie Mellon University, USA)

Panel Members: Satrajit Chatterjee (Two Sigma Investments, New York, USA), Petru Eles (Linkoping University, Sweden), Chenyang Lu (Washington University in St. Louis, USA), Karam Chatha (Qualcomm, USA), Partha Pande(Washington State University, USA), Radu Marculescu (Carnegie Mellon University, USA)

Over the years, ESWEEK has benefited from a clear target and a relatively homogeneous community of people interested in various hardware and/or software aspects. In recent years, however, the raise of new applications (bio, social, etc.) led inevitably to a possible shift in the overall focus towards embedded cyber-physical systems. However, it is hard to ignore the value of lessons learned when (co)designing HW and SW, or optimizing software and systems for utmost performance. Indeed, the kind of methods and tools we've seen presented over the years in ESWEEK form a solid intellectual legacy we can build on if we were to move into these new areas and design new kind of systems.

Starting from these overarching ideas, this special session/panel is meant to bring to discussion a set of outrageously cool (new) applications and explore an out-of-the-box perspective on systems design. The participants and audience alike will be challenged to leave the comfort zone (a.k.a. traditional embedded system design), travel the path not taken, see the unseen, and immerse into the joy of designing new "things". In the end, it will become clear what’s at stake for the embedded community as we want (or maybe need?) to reinvent ourselves...

Monday	CASES	EMSOFT	CODES+ISSS
0800 - 0830	**Opening Session**		
0830 - 0930	**Keynote: "System of Systems and Geography of Computing", Jaswinder S. Ahuja, Cadence**		
0930 - 1000	**Coffee Break**		
1000 - 1200	**Session 1: Multi-cores and Accelerators** *Session Chair: Weidong Shi*	**Session 1: Formal Modeling** *Session Chair: Rupak Majumdar*	**Session 1A: Networked Embedded Systems** *Session Chair: Lothar Thiele* *Session Co-Chair: Siddharth Garg*
	1.1 The Improbable but Highly Appropriate Marriage of 3D Stacking and Neuromorphic Accelerators *Olivier Temam, Bilel Belhadj, Alexandre Valentian, Pascal Vivet, Marc Duranton and Liqiang He*	**1.1 Exponentially timed SADF: Compositional semantics, reduction, and analysis** *Joost-Pieter Katoen and Hao Wu*	**1A.1: Hardware/Software Co-design for a Wireless Sensor Network Platform** *Chih-Ming Hsieh, Farzad Samie, M. Sammer Srouji, Manyi Wang, Zhonglei Wang and Joerg Henkel*
	1.2 Greedy Heuristics for Transport Triggered Architecture Optimization *Timo Viitanen, Heikki Kultala, Pekka Jääskeläinen and Jarmo Takala*	**1.2 Refinement Calculus of Reactive Systems** *Viorel Preoteasa and Stavros Tripakis*	**1A.2: Towards Scalable Symbolic Routing for Multi-Objective Networked Embedded System Design and Optimization** *Sebastian Graf, Felix Reimann, Michael Glaß and Jürgen Teich*
	1.3 Energy-Efficient VFI-Partitioned Multicore Design Using Wireless NoC Architectures *Ryan Kim, Guangshuo Liu, Paul Wettin, Radu Marculescu, Diana Marculescu and Partha Pande*	**1.3 Precise Piecewise Affine Models from Input-Output Data** *Rajeev Alur and Nimit Singhania*	**1A.3: An Efficient Technique for Computing Importance Measures in Automatic Design of Dependable Embedded Systems** *Hananeh Aliee, Michael Glass, Faramarz Khosravi and Jürgen Teich*
1000 - 1200			**Session 1B: Efficient, Reliable and Secure Architectures** *Session chair: Muhammad Shafique* *Session Co-Chair: Petru Eles*
			1B.1: HEFT: A Hybrid System-Level Framework for Enabling Energy-Efficient Fault-Tolerance in NoC based MPSoCs *Yong Zou and Sudeep Pasricha*
			1B.2: Leveraging Microarchitectural Side Channel Information to Efficiently Enhance Program Control Flow Integrity *Chen Liu and Chengmo Yang*
			1B.3: *A PCM Translation Layer for Integrated Memory and Storage Management *Bing-Jing Chang, Yuan-Hao Chang, Hung-Sheng Chang, Tei-Wei Kuo and Hsiang-Pang Li*
1200 - 1300	**Lunch**		

Monday	CASES	EMSOFT	CODES+ISSS
1300 - 1500	**Session 2: Reconfigurable Computing** *Session chair: Alexander Fell*	**Session 2: Special Session: Embedded Software Reliability for Unreliable Hardware** *Organizers: Muhammad Shafique and Jian-Jia Chen* *Moderator: Sri Parameswaran*	**Session 2A: Energy/Performance Optimization and Timing Error Modeling** *Session Chair: Chengmo Yang* *Session Co-Chair: Turbo Majumder*
	2.1 Retargetable Automatic Generation of Compound Instructions for CGRA based Reconfigurable Processor Applications *Narasinga Rao Miniskar, Soma Kohli, Haewoo Park and Donghoon Yoo*	**Speakers:** **1. Peter Marwedel** **2. Nikil Dutt** **3. Rolf Ernst** **4. Jian-Jia Chen** **5. Siddharth Garg**	**2A.1: Timing Analysis of Erroneous Systems** *Omid Assare and Rajesh Gupta*
	2.2 *COREFAB: Concurrent Reconfigurable Fabric Utilization in Heterogeneous Multi-Core Systems *Artjom Grudnitsky, Lars Bauer and Jörg Henkel*		**2A.2: Saving Energy without Defying Deadlines on Mobile GPU-based Heterogeneous Systems** *Arian Maghazeh, Unmesh D. Bordoloi, Adrian Horga, Petru Eles and Zebo Peng*
	2.3 Automatic Custom Instruction Identification in Memory Streaming Algorithms *Martin Haaß, Lars Bauer and Joerg Henkel*		**2A.3: Flattening-based Mapping of Imperfect Loop Nests for CGRAs** *Jongeun Lee, Seongseok Seo, Hongsik Lee, and Hyeon Uk Sim*
1300 - 1500			**Session 2B: Pushing the Boundaries – Temperatures, Voltages, and Cloudbursts** *Session Chair: M. Balakrishnan* *Session Co-Chair: Aviral Shrivastava*
			2B.1: *TSP: Thermal Safe Power - Efficient power budgeting for Many-Core Systems in Dark Silicon *Santiago Pagani, Heba Khdr, Waqaas Munawar, Jian-Jia Chen, Muhammad Shafique, Minming Li and Joerg Henkel*
			2B.2: HYPNOS: An Ultra-Low Power Sleep Mode with SRAM Data Retention for Embedded Microcontrollers *Hrishikesh Jayakumar, Arnab Raha and Vijay Raghunathan*
			2B.3: Prediction and Control of Bursty Cloud Workloads: A Fractal Framework *Mahboobeh Ghorbani, Yanzhi Wang, Massoud Pedram and Paul Bogdan*
1500 - 1530	**Coffee Break**		

Monday	CASES	EMSOFT	CODES+ISSS
1530 - 1730	**Session 3A: Parallel Programming Frameworks** *Session chair: Oliver Bringmann*	**Session 3: Testing and Validation** *Session Chair: Nicolas Halbwachs*	**Session 3: Special Session: Dark Silicon as a Challenge for Hardware-Software Codesign** *Organizers: Mohammad Shafique and Siddharth Garg*
	3A.1 Auto-parallelization of Data Structure Operations for GPUs *Rupesh Nasre*	**3.1 *Multiple Shooting, CEGAR-based Falsification for Hybrid Systems** *Aditya Zutshi, Sriram Sankaranarayanan, Jyotirmoy V. Deshmukh, James Kapinski*	**3.1 The Dark Silicon Problem: Introduction, Challenges and Opportunities** *Jörg Henkel*
	3A.2 A Novel Compilation Flow for Parametric Dataflow: Programming Model, Scheduling, and Application to Heterogeneous MPSoC *Mickaël Dardaillon, Kevin Marquet, Tanguy Risset, Jérôme Martin and Henri-Pierre Charles*	**3.2 SiPTA: Signal Processing for Trace-based Anomaly Detection** *Mohammad Mehdi Zeinali, Mahmoud Salem, Neeraj Kumar, Greta Cutulenco, Sebastian Fischmeister*	**3.2 Synthesizing Heterogeneous Dark Silicon Processors** *Siddharth Garg*
	3A.3 *A Compiler Framework for Automatically Mapping Data Parallel Programs to Heterogeneous MPSoCs *Kiran Chandramohan and Michael F.P. O'Boyle*	**3.3 Blaming in Component-Based Real-Time Systems** *Gregor Goessler and Lacramioara Astefanoaei*	**3.3 On-Chip Networks for Dark Silicon Processors** *Sri Parameswaran*
			3.4 Run-Time Management of Heterogeneous Dark Silicon Processors *Tulika Mitra*
1530 - 1730	**Session 3B: Memory Systems** *Session Chair: Aviral Shrivastava*		
	3B.1 Team Up: Cooperative Memory Management in Embedded Systems *Isabella Stilkerich, Philip Taffner, Christoph Erhardt, Christian Dietrich, Christian Wawersich and Michael Stilkerich*		
	3B.2 A Low-Cost Memory Interface for High-Throughput Accelerators *Jing Huang, Yuanjie Huang, Yunji Chen, Paolo Ienne, Olivier Temam and Chengyong Wu*		
	3B.3 EnVM : Virtual Memory Design for New Memory Architectures *Pooja Roy, Manmohan Manoharan and Weng Fai Wong*		
1800-1845	**Cultural Program**		

Tuesday	CASES	EMSOFT	CODES+ISSS
0830 - 0930	**Keynote: "Emerging Trends in Electronics in an Intelligent Connected World", Guru Ganesan, ARM**		
0930 - 1000	**Coffee Break**		
1000 – 1200	**Session 4: Simulation & Validation** *Session Chair: Apala Guha*	**Session 4A: Software Timing Analysis** *Session chair: Wang Yi*	**Session 4: QoS for Large-scale Systems** *Session Chair: Jürgen Teich* *Session Co-Chair: Smruti Sarangi*
	4.1 A System-level Simulation Framework for Evaluating Task Migration in MPSoCs *Wei Quan and Andy Pimentel*	**4A.1 A General Approach for Expressing Infeasibility in Implicit Path Enumeration Technique** *Pascal Raymond*	**4.1: Job Arrival Rate Aware Scheduling for Asymmetric Multi-core Servers In the Dark Silicon Era** *Bharathwaj Raghunathan and Siddharth Garg*
	4.2 *Context-Sensitive Timing Simulation of Binary Embedded Software *Sebastian Ottlik, Stefan Stattelmann, Alexander Viehl, Oliver Bringmann and Wolfgang Rosenstiel*	**4A.2 Computing Maximum Blocking Times with Explicit Path Analysis under Non-local Flow Bounds** *Jan Kleinsorge and Peter Marwedel*	**4.2: Improving Formal Timing Analysis of Switched Ethernet by Exploiting Traffic Stream Correlations** *Daniel Thiele, Philip Axer, Rolf Ernst and Jan Reinke Seyler*
	4.3 Automated ISA Branch Coverage Analysis and Test Case Generation for Retargetable Instruction Set Simulators *Harry Wagstaff, Tom Spink and Björn Franke*	**4A.3 Extending Typical Worst-Case Analysis Using Response-Time Dependencies to Bound Deadline Misses** *Zain A. H. Hammadeh, Sophie Quinton, Rolf Ernst*	**4.3: *Tackling QoS-induced Aging in Exascale Systems through Agile Path Selection** *Dean Michael Ancajas, Koushik Chakraborty, Sanghamitra Roy and Jason Allred*
1000 - 1200		**Session 4B: Energy** *Session Chair: Zili Shao*	
		4B.1 Energy Efficient DVFS Scheduling for Mixed-Criticality Systems *Pengcheng Huang, Pratyush Kumar, Georgia Giannopoulou, Lothar Thiele*	
		4B.2 p-YDS Algorithm: An Optimal Extension of YDS Algorithm to Minimize Expected Energy For Real-Time Jobs *Pratyush Kumar and Lothar Thiele*	
		4B.3 Robust Strategy Synthesis for Probabilistic Systems Applied to Risk-Limiting Renewable-Energy Pricing *Alberto Puggelli, Alberto Sangiovanni-Vincentelli, Sanjit Seshia*	
1200 - 1300	**Lunch**		
1300 - 1500	**Session 5: Special Session – Embedded Platforms for the Internet of Things** *Session chair: Ravi Iyer*	**Session 5A: Synthesis** *Session Chair: Sanjit A. Seshia*	**Session 5: High-level Design Techniques** *Session Chair: Andy Pimentel* *Session Co-Chair: Akash Kumar*
	5.1: Embedded system architectures for wearable physiological and inertial sensing *Kumar Ranganthan*	**5A.1 *Deductive Control Synthesis for Alternating-Time Logics** *Rayna Dimitrova and Rupak Majumdar*	**5.1: Code Generation from a Domain-specific Language for C-based HLS of Hardware Accelerators** *Oliver Reiche, Moritz Schmid, Frank Hannig, Richard Membarth and Jürgen Teich*

Tuesday	CASES	EMSOFT	CODES+ISSS
	5.2: Powering the Internet of Things *Vijay Raghunathan*	**5A.2 Infinite Horizon Safety Controller Synthesis through Disjunctive Polyhedral Abstract Interpretation.** *Hadi Ravanbakhsh and Sriram Sankaranarayanan*	**5.2: System-Level Memory Optimization for High-Level Synthesis of Component-Based SoCs** *Christian Pilato, Paolo Mantovani, Giuseppe Di Guglielmo and Luca Carloni*
		5A.3 Synthesising Optimal Timing Delays for Timed I/O Automata *Marco Diciolla, Peter Kim, Marta Kwiatkowska, Alexandru Mereacre*	**5.3: Policy-based Message Scheduling Using FlexRay** *Philipp Mundhenk, Florian Sagstetter, Sebastian Steinhorst, Martin Lukasiewycz and Samarjit Chakraborty*
1300 – 1500		**Session 5B: Multi-threading** *Session Chair: Dionisio de Niz*	
		5B.1 Automated Software Testing of Memory Performance in Embedded GPUs Sudipta Chattopadhyay, Petru Eles, Zebo Peng	
		5B.2 On the Existence of Probe Effect in Multi-threaded Embedded Programs Young Wn Song and Yann-Hang Lee	
		5B.3 Can We Put Concurrency Back into Redundant Multithreading? Bjoern Doebel and Hermann Härtig	
1500 - 1530	**Coffee Break**		
1530 - 1730	**Session 6: Compiler Optimization** *Session chair: Henri-Pierre Charles*	**Session 6A: Scheduling** *Session Chair: Lothar Thiele*	**Session 6: Special Session: Self-Awareness in Cyber Physical Systems** *Organizers: Kalle Tammemae and Axel Jantsch*
	6.1 Control-Layer Optimization for Flow-Based mVLSI Microfluidic Biochips *Kai Hu, Trung Anh Dinh, Tsung-Yi Ho and Krishnendu Chakrabarty*	**6A.1 *Schedulability Analysis of Global Memory-Predictable Scheduling** *Ahmed Alhammad and Rodolfo Pellizzoni*	**6.1 A Framework of Awareness for Artificial Subjects** *Axel Jantsch, Kalle Tammemae*
	6.2 Splitting Functions into Single-Entry Regions *Stefan Hepp and Florian Brandner*	**6A.2 Supporting Read/Write Applications in Embedded Systems via I/O placement and suspension-aware analysis** *Guangmo Tong and Cong Liu*	**6.2 Generating Situation Awareness in Cyber-Physical Systems: Creation and Exchange of Situational Information** *Jürgo-Sören Preden*
	6.3 GCCFG: A New Graphical Representation for Inter-procedural Optimization for Software Managed Manycore (SMM) Architectures *Bryce Holton, Aviral Shrivastava, Ke Bai and Harini Ramaprasad*	**6A.3 Task Mapping in Heterogeneous Embedded Systems for Fast Completion Time** *Husheng Zhou and Cong Liu*	**6.3 On-Chip Self-Awareness Using Cyberphysical-Systems-On-Chip (CPSoC)** *Santanu Sarma, Nikil Dutt, P. Guptay, Alex Nicolau, Nalini Venkatasubramanian*
			6.4 From Self-Aware Building Blocks to Self-Organizing Systems with Hierarchical Agent-based Adaptation *Liang Guang, Juha Plosila and Hannu Tenhunen*

Tuesday	CASES	EMSOFT	CODES+ISSS
1530 - 1730		**Session 6B: Cyber-Physical Systems** *Session Chair: Todor Stefanov*	
		6B.1 Contract-Based Integration of Cyber-Physical Analyses *Ivan Ruchkin, Dionisio de Niz, Sagar Chaki, David Garlan*	
		6B.2 CPSGrader: Synthesizing Temporal Logic Testers for Auto-Grading an Embedded Systems Laboratory *Alexandré Donze, Garvit Juniwal1, Jeff C. Jensen, Sanjit A. Seshia*	
		6B.3 Real-Time System Support for Hybrid Structural Simulation *David Ferry, Kunal Agrawal, Chris Gill, Chenyang Lu, Gregory Bunting, Amin Megareh, Shirley Dyke, Arun Prakash*	
1800 - 2100	**Reception, Keynote: "Simulation is Passé; all Future Systems Require FPGA Prototyping", Prof. Arvind, MIT, and Banquet**		

Wednesday	CASES	EMSOFT	CODES+ISSS
0830 - 0930	**Keynote: "Smart energy: Ubiquitous Role of Embedded Systems", Prof. Krithi Ramamritham, IITB**		
0930 - 1000	**Coffee Break**		
1000 - 1200	**Session 7: Energy Efficiency** *Session Chair: Anshul Kumar*	**Session 7: Multi- and Many-core Integration** *Session Chair: Cong Liu*	**Session 7A: System Simulation and Validation** *Session Chair: Mark Zwolinski* *Session Co-Chair: Lava Bhargava*
	7.1 CAPED: Context-aware Personalized Display Brightness for Mobile Devices *Matthew Schuchhardt, Susmit Jha, Raid Ayoub, Michael Kishinevsky and Gokhan Memik*	**7.1 Parallel Many-Core Avionics Systems** *Milos Panic, Eduardo Quinones, Pavel Zaykov, Carles Hernandez, Jaume Abella, Francisco Cazorla*	**7A.1: Metronomy: A Function-Architecture Co-simulation Framework for Timing Verification of Cyber-Physical Systems** *Liangpeng Guo, Qi Zhu, Pierluigi Nuzzo, Roberto Passerone, Alberto Sangiovanni-Vincentelli and Edward Lee*
	7.2 A high-level model of embedded flash energy consumption *James Pallister, Kerstin Eder, Simon Hollis and Jeremy Bennett*	**7.2 Real-Time Multi-Core Virtual Machine Scheduling in Xen** *Sisu Xi, Meng Xu, Chenyang Lu, Linh Phan, Christopher Gill, Oleg Sokolsky, Insup Lee*	**7A.2: Automated Firmware Testing using Firmware-Hardware Interaction Patterns** *Sunha Ahn and Sharad Malik*
	7.3 Reducing Cache Leakage Energy for Hybrid SPM-Cache Architectures *Hao Wen and Wei Zhang*	**7.3 EDF as an Arbitration Policy for Wormhole-Switched Priority-Preemptive NoCs -- Myth or Fact?** *Borislav Nikolic and Stefan M. Petters*	**7A.3: HSAemu – A Full System Emulator for HSA Platforms** *Jiun-Hung Ding, Wei-Chung Hsu, Bai-Cheng Jeng, Shih-Hao Hung and Yeh-Ching Chung*
1000 – 1200			**Session 7B: Embedded Security and Automotives** *Session Chair: Axel Jantsch* *Session Co-Chair: Oliver Bringmann*
			7B.1: System-of-PUFs: Multilevel Security for Embedded Systems *Sven Tenzing Choden Konigsmark, Leslie Hwang, Deming Chen and Martin Wong*
			7B.2: A Low Cost Acceleration Method for Hardware Trojan Detection Based on Fan-out Cone Analysis *Bin Zhou, Wei Zhang and Srikanthan Thambipillai*
			7B.3: RunPar: An Allocation Algorithm for Automotive Applications Exploiting Runnable Parallelism in Multicores *Milos Panic, Sebastian Kehr, Eduardo Quinones, Bert Boeddeker, Jaume Abella and Francisco Cazorla*
1200 – 1300	**Lunch**		
1300 – 1500	**Session 5: Resilience** *Session Chair: Akash Kumar*	**Session 8. Memory and I/O** *Session chair: Aviral Shrivastava*	**Session 8A: Energy Capture and Storage** *Session Chair: Soonhoi Ha* *Session Co-Chair: Sungjoo Yoo*
	5.1 AdaPNet: Adapting Process Networks in Response to Resource Variations *Lars Schor, Iuliana Bacivarov, Hoeseok Yang and Lothar Thiele*	**8.1 DriverGen: Automating the Generation of Serial Device Drivers** *Jiannan Zhai1, Yuheng Du, Shiree Hughes, Jason Hallstrom*	**8A.1: Verification of Balancing Architectures for Modular Batteries** *Martin Lukasiewycz, Sebastian Steinhorst and Swaminathan Narayanaswamy*

	5.2 SDCTune: A Model for Predicting the SDC-Proneness of an Application for Configurable Protection *Qining Lu, Karthik Pattabiraman, Meeta S Gupta and Jude A Rivers*	**8.2 Building High-Performance Smartphones via Non-Volatile Memory: The Swap Approach** Kan Zhong, Tianzheng Wang, Xiao Zhu, Linbo Long, Duo Liu, Weichen Liu, Zili Shao, Edwin Sha	**8A.2: Cost-Effective Design of a Hybrid Electrical Energy Storage System for Electric Vehicles** *Di Zhu, Siyu Yue, SangYoung Park, Yanzhi Wang, Naehyuck Chang and Massoud Pedram*
	5.3 Scalable and Fault Resilient Physical Neural Networks on a Single Chip *Weidong Shi, Yuanfeng Wen, Ziyi Liu, Xi Zhao, Dainis Boumber, Ricardo Vilalta and Lei Xu*		**8A.3: Fault-Aware Application Scheduling in Low Power Embedded Systems with Energy Harvesting** *Yi Xiang and Sudeep Pasricha*
1300 – 1500			**Session 8B: Scheduling** *Session Chair: Fadi Kurdahi* *Session Co-Chair: Christian Pilato*
			8B.1: 3M-PCM: Exploiting Multiple Write Modes MLC Phase Change Main Memory in Embedded Systems *Chen Pan, Mimi Xie, Jingtong Hu, Yiran Chen and Chengmo Yang*
			8B.2: DAARM: Design-Time Application Analysis and Run-Time Mapping for Predictable Execution in Many-Core Systems *Andreas Weichslgartner, Deepak Gangadharan, Stefan Wildermann, Michael Glaß and Jürgen Teich*
			8B.3: Workload-aware Shaping of Shared Resource Accesses in Mixed-criticality Systems *Sebastian Tobuschat, Moritz Neukirchner, Leonardo Ecco and Rolf Ernst*
1500 -1530	**Coffee Break**		
1530 - 1730	**ESWEEK at Crossroads: New Applications, New Challenges, and the Road Ahead Toward Designing New "Things"** **Panel Members: Satrajit Chatterjee (Two Sigma Investments, New York, USA), Petru Eles (Linkoping University, Sweden), Chenyang Lu (Washington University in St. Louis, USA), Karam Chatha (Qualcomm, USA), Partha Pande(Washington State University, USA), Radu Marculescu (Carnegie Mellon University, USA)**		
1730 - 1745	**Closing and Best Paper Awards**		