EMBEDDED SYSTEMS WEEK

Conference Program

ESWEEK.ORG
OCTOBER 4-9, 2015
AMSTERDAM

SPONSORED BY:

acm IEEE

Welcome to ESWEEK 2015 in Amsterdam!

Embedded Systems Week (ESWEEK) is the premier event covering all aspects of embedded systems and software. By bringing together three leading conferences (CASES, CODES+ISSS, and EMSOFT), three symposia (ESTIMedia, IoT, and RSP) and several workshops and tutorials, ESWEEK allows attendees to benefit from the whole range of embedded system topics in research and development.

The 21 regular sessions with three papers each are complemented by 7 invited sessions focusing on new research trends or challenges. The regular sessions and special sessions of the three conferences are organized in four parallel tracks. There is a strong emphasis on interaction: At the end of each session, there is a poster presentation during which all presented papers are discussed with the authors. As always, the paper selection process has been very competitive with acceptance ratios of 35% for CASES, 26.6% for CODES+ISSS and 25.9% for EMSOFT.

This year, there will be 4 distinguished industrial and academic keynotes highlighting important trends moving or even shaking the industry, all enabled by embedded systems and with strong influence on embedded systems design. In his keynote “Enabling the digital transformation for a smarter life,” Philippe Magarshak, CTO Embedded Processing Solutions of ST Microelectronics and President of the Minalogic Collaborative R&D Cluster, will talk about the upcoming challenges and opportunities of the Internet-of-Things. Michael Fausten, VP Vehicle Systems Development at Bosch, will ask “Evolution or Revolution?” when he elaborates the ”Requirements for the architecture of automated vehicles”. Manfred Morari, professor at ETH Zuerich, and one of the most prominent researchers in automated control will demonstrate the importance of embedded system performance for cyber-physical systems in the keynote “Fast Model Predictive Control”. In his keynote “Connected Vehicles-Cars talking to each other, safe & securely”, Mark Steigemann, Senior Director Product Architecture, NXP Business Unit Automotive, will address another hot trend, the opening of previously closed embedded system domains and its impact on systems architecture and design. All these keynotes demonstrate that embedded systems are at the core of industrial and societal developments, more influential than ever, in an environment of highly active research.

The three conferences will close with a plenary panel “Embedded System Security - What does it change?” targeting a controversial topic, the best way to approach security issues. Top experts from academia and industry will share their views on security and discuss research topic priorities, the cost of security and who is willing to pay for it or possibly accept reduced comfort.

Thursday and Friday are the days for symposia and workshops. The two established symposia, ESTIMEDIA (Real-time Multimedia) and RSP (Rapid System Prototyping), which have been part of ESWEEK for many years, are now accompanied by a third, new symposium on the Internet-of-Things. The Workshop on Design, Modeling and Evaluation of Cyber Physical Systems, CyPhy, is an established event that has joined ESWEEK for the first time, just like the Embedded Operating Systems Workshop, EWiLi. WESE (education) and WESS (security) have been with ESWEEK for a while. There is one new workshop on Resiliency in Embedded Electronic Systems, REES, that is organized for the first time.

The Sunday tutorials preceding the conferences have always been an excellent opportunity to get in-depth knowledge in new trends. This year, the tutorials will cover security attacks via memory, the use and benefits of meta-modeling in system-level design automation, probabilistic timing analysis, mixed criticality systems and monitor design for cyber-physical systems.

The organization was only possible due to the help of many volunteers, the program chairs with their program committee members, the organizers of workshops, tutorials and symposia, all members of the organizing committee, the local arrangement chairs and their helpers, and the conference secretariat. We would like to thank everyone for their support! The best reward will be a successful event.

ESWEEK will be held right in the center of Amsterdam, at a spectacular site right at the waterfront of the river IJ. We look forward very much to meeting you there!

Rolf Ernst
General Chair

Jörg Henkel
Vice General Chair

Table of Contents

Conference Venue

Mövenpick Hotel Amsterdam City Centre

Piet Heinkade 11 | 1019 BR Amsterdam | The Netherlands
+31 (0) 20 519 1200 | hotel.amsterdam@moevenpick.com
http://www.moevenpick-hotels.com/en/europe/netherlands/amsterdam/hotel-amsterdam/overview/

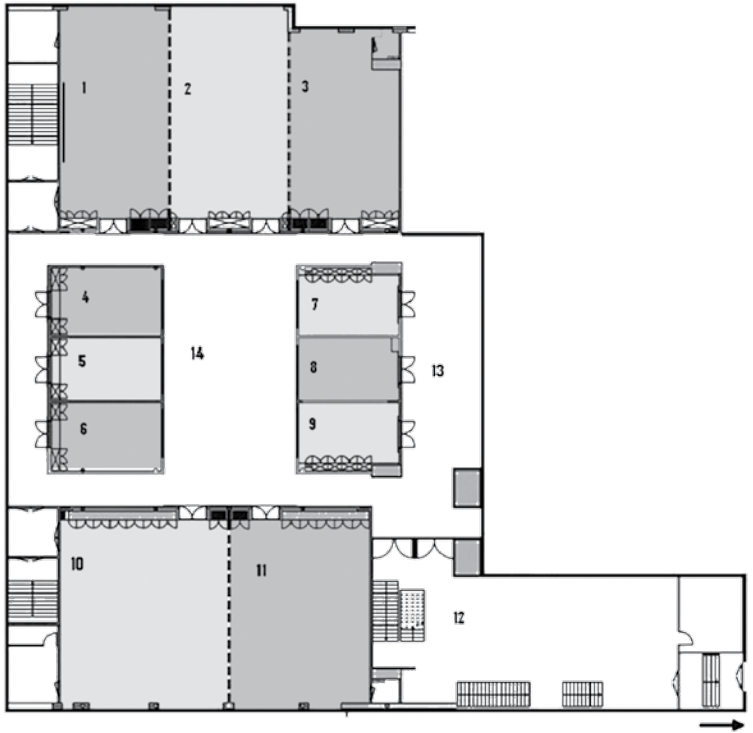
The hotel is located alongside the water's edge of the river IJ in the vibrant heart of Amsterdam and can easily be reached via multiple forms of transport. Amsterdam Central Station (Amsterdam Centraal in Dutch) is walking distance from Mövenpick Hotel Amsterdam City Centre and the hotel also offers a complimentary shuttle bus. Please book your seats in advance at the hotel's concierge desk: +31 (0)20 519 1213.

The direct train from Schiphol Amsterdam Airport (AMS) to Amsterdam Central Station takes 20 minutes and by taxi to the hotel is around 30 minutes. The "Muziekgebouw/ Bimhuis" tram stop is in front of the hotel, which is adjacent to the Passenger Cruise Terminal. Canal boats and water taxis can stop in front of the hotel at the hotel's own jetty.

For a more detailed route description to the hotel look at:
http://www.moevenpick-hotels.com/en/europe/netherlands/amsterdam/hotel-amsterdam/location

1. Matterhorn I
2. Matterhorn II
3. Matterhorn III
4. Basel
5. Luzern
6. Geneva
7. Lausanne
8. St. Gallen
9. Winterthur
10. Zürich II
11. Zürich I
12. Foyer I
13. Foyer II
14. Atrium Foyer

Conference Venue Floorplan



Hotel Reservations

Mövenpick Hotel Amsterdam City Centre offers special prices for ESWeek delegates with the following booking code: ESWeek 2015. To book a room in the hotel, please use the following link:
https://gc.synxis.com/rez.aspx?Hotel=15718&Chain=7714&arrive=10%2f4%2f2015&depart=10%2f9%2f2015&adult=1&child=0&group=ESWeek+2015.

Use the above link and choose the dates you would like to stay at the hotel. The booking code will be in the box Group Code, automatically. Without using the above link, you need to use the Booking Code and enter this in the Box Group code, manually: **https://gc.synxis.com/rez.aspx?Hotel=15718&Chain =7714&arrive= 10%2f4%2f2015&depart= 10%2f9%2f2015&adult 1&child=0&group=ESWeek+2015**.

It is also possible to send your requirements, personal details and credit card info to the hotel's reservation department, so they can book the rooms for you. You can reach them by e-mail: hotel.amsterdam@moevenpick.com or by phone: +31 (0)20 519 1234. Please use the group code ESWeek 2015 to make your reservation.

Other hotels: Amsterdam offers 400 hotels in the city center (700 in the whole city) at different price ranges: Low-budget: <100 Euro/night; 3-4 stars: 100-250 Euro/night; and 5 stars: > 250 Euro/night. Just use Booking.com or other similar websites to select your preferred hotel and book a room.

2015 ESWeek Proceedings Distribution

ESWeek Proceedings will be delivered electronically online via a username and password.

To access: **http://esweekproceedings.mpassociates.com**
Username = Email address that you registered with
Password = Registration ID (on your badge)
The download site will close at 5:00pm (MST) on Tuesday, October 13, 2015. After this date, the ESWeek Proceedings will be available in the ACM and IEEE digital libraries.

Registration and Information Desk

Location: Foyer I

Operating Hours:

Sunday, October 4	08:00 – 17:30
Monday, October 5	08:00 – 17:30
Tuesday, October 6	08:00 – 17:30
Wednesday, October 7	08:00 – 17:30
Thursday, October 8	08:00 – 17:30
Friday, October 9	08:00 – 12:30

Conference Registration Fees

Conference registration allows attendance to any of the three ESWEEK conferences, includes lunch on conference days, online conference proceedings, the Sunday Welcome Reception and the Tuesday Evening Canals Boat Tour and Banquet. All fees include 21% VAT.

	ADVANCE RATE SEPTEMBER 8, 2015		RATE AFTER SEPTEMBER 8, 2015	
	IEEE OR ACM MEMBER	NON MEMBER	IEEE OR ACM MEMBER	NON MEMBER
Conference Only	€725	€865	€900	€1080
Student Conference Only	€515	€620	€640	€775

Registration Fees: Tutorials

Tutorials can be added to your conference registration for additional fees.
Tutorial participants must register for each tutorial they would like to attend. All fees include 21% VAT.

	ADVANCE RATE SEPTEMBER 8, 2015		RATE AFTER SEPTEMBER 8, 2015	
	IEEE OR ACM MEMBER	NON MEMBER	IEEE OR ACM MEMBER	NON MEMBER
Full Day				
Tutorial 1	€215	€265	€265	€330
Tutorial 2	€215	€265	€265	€330
Half Day Morning				
Tutorial 3	€105	€125	€135	€155
Half Day Afternoon				
Tutorial 4	€105	€125	€135	€155
Tutorial 5	€105	€125	€135	€155

Registration Fees: Evening Banquet

The banquet evening event will be held on Tuesday, October 6, 2015. Banquet is included in the regular Conference Registration. Additional guest banquet dinner tickets may be purchased. All fees include 21% VAT.

	ADVANCE RATE SEPTEMBER 8, 2015	RATE AFTER SEPTEMBER 8, 2015
Guest Banquet Ticket	€120	€120

Registration Fees: Workshops

Workshops can be added to your conference registration for additional fees.
Participants must register for each workshop they would like to attend. All fees include 21% VAT.

	ADVANCE RATE SEPTEMBER 8, 2015		RATE AFTER SEPTEMBER 8, 2015	
	IEEE OR ACM MEMBER	NON MEMBER	IEEE OR ACM MEMBER	NON MEMBER
Workshop 1	€215	€265	€265	€330
Workshop 2	€215	€265	€265	€330
Workshop 3	€215	€265	€265	€330
Workshop 4	€215	€265	€265	€330
Workshop 5	€215	€265	€265	€330

Registration Fees: Symposia

Symposia can be added to your conference registration for additional fees.
Attendees must register for each symposium they would like to attend. All fees include 21% VAT.

	ADVANCE RATE SEPTEMBER 8, 2015		RATE AFTER SEPTEMBER 8, 2015	
	IEEE OR ACM MEMBER	NON MEMBER	IEEE OR ACM MEMBER	NON MEMBER
Thursday, October 8				
IoT Symposium	€215	€265	€265	€330
Thursday & Friday October 8 - 9, 2015				
ESTIMedia Symposium	€300	€355	€375	€440
RSP Symposium	€300	€355	€375	€440

Travel to Amsterdam

The Schiphol Amsterdam Airport (http://www.schiphol.nl/index_en.html) is the 4th-largest air traffic hub in Europe. So, flying into Amsterdam should be easy wherever you are. Schiphol airport has a railway station right underneath the terminal building. Trains to Amsterdam Central Station (http://en.wikipedia.org/wiki/Amsterdam_Centraal_railway_station) depart every few minutes and take 15-20 minutes for less than 5 EUR. Taking a taxi is usually not a good idea: taxis are very expensive and much slower than trains. Taking a taxi from Amsterdam Central Station to your hotel may be an option, still expensive compared with other countries though.

High speed rail services connect Amsterdam to Brussels (1h50), Paris (3h15), Cologne (2h30) and Frankfurt (4h00). Direct trains from Hannover and Berlin, sleeper services from Copenhagen, Berlin, Warsaw, Moscow, Prague, Munich and Zurich or the overnight ferry (http://www.dfdsseaways.com) from Newcastle can be further alternatives to air travel. See Thalys (http://www.thalys.com) for connections from Belgium and France, Deutsche Bahn (http://www.bahn.de/i/view/GBR/en/index.shtml) for connections from Germany and the rest of Europe or Nederlandse Spoorwegen (Dutch Railways http://www.ns.nl/en) for domestic rail services.

Getting Around in Amsterdam

With about 800,000 inhabitants, Amsterdam is by far the largest city in The Netherlands, but certainly one of the smaller capital cities in the world. Large parts of the historic center date back to the 17th and 18th century making Amsterdam an open-air museum inviting you to stroll alongside the famous canals. Unless you have mobility issues, almost any distance in the historic center of Amsterdam, which can easily be identified on a map as anything inside the outermost canal ring, may be considered walking distance.

Notwithstanding, a large number of tram lines as well as a few bus lines criss-cross central Amsterdam with Amsterdam Central Station (Amsterdam Centraal in Dutch) being the main hub of exchange. Tickets are available from either the tram driver (enter at the front of the tram or bus) or better from the conductor (enter at the rear part of the tram). Single tickets are fairly expensive. If you plan to make more extensive use of public transport within Amsterdam, there are attractive 24/48/72-hour tickets available from vending machines at Amsterdam Centraal metro station or the GVB office opposite the main entrance of Amsterdam Central Station. All tickets are interoperable between tram, metro and city buses.

See local transport operator GVB at http://en.gvb.nl/ for more details.

Local Attractions

One of the most popular travel destinations in Europe, Amsterdam is a compact, charming and cosmopolitan city that deserves exploration. Known as the "Venice of the North" for its more than 100 canals, the capital of The Netherlands offers easy sightseeing adventures by foot, bike, or boat. From the city's fine art museums to its colorful flower markets, from cannabis-selling "coffee shops" to the red light district, there's something exciting and unique to discover in Amsterdam at every turn. Nevertheless, there are places in the city you should not miss during your visit.
Here is our list of the best of the best.

Canals of Amsterdam

The famous canals were built during the 17th century to control the flow of the Amstel River and to add acres of dry land to the city. Amsterdam's wealthy merchants soon discovered that the canals were ideal for showcasing their mansions as well. A boat or bike ride along the city's 100 canals offers visitors a relaxing way to view traditional Dutch architecture.

Rijksmuseum

The Rijksmuseum is the largest and the most attractive museum in The Netherlands, with more than one million visitors each year. The museum has a wonderful collection of the 17th century Dutch Golden Age masterpieces; the famous "The Night Watch" by Rembrandt as well as other celebrated paintings like Vermeer's "The Milkmaid" and "Woman reading a letter", "The Windmill at Wijk bij Duurstede" by van Ruisdael, "The Burgomaster of Delft and his Daughter" by Jan Steen and many more. Unique sculptures and various antiquities as traditional furniture, Delftware, silver, ship models, and doll houses complete the show.

Van Gogh Museum

This modern museum houses some 200 paintings and 550 sketches showing Van Gogh in all his moods. This biggest in the world collection, combined with hundreds of letters by Van Gogh, and selected works by his friends and contemporaries, form the core of the museum's collection.

Anne Frank House

Amsterdam's most visited attraction, the Anne Frank Huis is situated along the Prinsengracht canal. The structure that once hid Anne Frank, her family, and four other Jewish people from the Nazi authorities during World War II has been viewed as a memorial to the Holocaust since 1947, when Anne's father published the world-famous diary that Anne wrote while they lived hidden within the building.

Bloemenmarkt

The Bloemenmarkt is the world's only floating flower market. Seven days a weeks, flower sellers load stands and floating barges with all of the flowers and bulbs for which The Netherlands is famous. Founded in 1862, the Bloemenmarkt includes more than a dozen different florists and garden shops as well as souvenir stalls.

De Wallen

De Wallen is Amsterdam's famous red-light district, the city's designated area for legalized prostitution. More than one hundred one-room apartments are rented by sex workers who entice onlookers from behind windows illuminated with red lights. A strong police presence keeps the neighborhood very safe. Although taking pictures is not allowed, tourists are welcome. As the oldest section in Amsterdam, the district is also home to several historic buildings, including the city's oldest church, the Gothic-style Oude Kerk.

Social Program

Welcome Reception

Date: Sunday, October 4, 2015
Time: 18:00 – 20:00
Location: Mövenpick Hotel Amsterdam City Centre – Atrium Foyer and Foyer I

Remarks: All registered ESWeek attendees are cordially invited. All attendees are requested to bring the ESWeek 2015 badges.

Amsterdam Canals Boat Tour

Date: Tuesday, October 6, 2015
Time: 17:30 – 18:00 Boarding on the boats
18:00 – 19:00 Boat tour
19:00 Boat tour ends and attendees are dropped off at the Banquet location (Westerkerk)

Location: The meeting point to board the boats and other relevant information will be provided at the ESWeek 2015 opening session.

Remarks: All registered ESWeek attendees are cordially invited. All attendees are requested to bring the ESWeek 2015 badges.

Conference Banquet Gala

Date: Tuesday, October 6, 2015
Time: 19:00 – 22:30
Location: Westerkerk Amsterdam, Prinsengracht 281, 1016 GW AMSTERDAM (http://www.westerkerk.nl/english)

Remarks: All registered ESWeek attendees are cordially invited.
All attendees are requested to bring the ESWeek 2015 badges.
Extra banquet coupons (for family members, etc.) could be purchased at the ESWeek Registration and Information Desk.

Best Paper Candidates

BEST PAPER COMMITTEE CHAIR

Petru Eles - *Linköping University*

CASES

5.1 Vector-Aware Register Allocation for GPU Shader Processors

Authors: Yi-Ping You - *National Chiao Tung Univ.*
Szu-Chieh Chen - *National Chiao Tung Univ.*

6.1 Efficient SAT-based Application Mapping and Scheduling on Multiprocessor Systems for Throughput Maximization

Authors: Weichen Liu - *Chongqing Univ.*
Zonghua Gu - *Zhejiang Univ.*
Yaoyao Ye - *Shanghai Jiao Tong Univ.*

6.3 High Performance and Energy Efficient Wireless NoC-Enabled Multicore Architecture for Graph Analytics

Authors: Karthi Duraisamy - *Washington State Univ.*
Hao Lu - *Washington State Univ.*
Partha Pande - *Washington State Univ.*
Ananth Kalyanaraman - *Washington State Univ.*

CODES+ISSS

1.1 R2Cache: Reliability-Aware Reconfigurable Last-Level Cache Architecture for Multi-Cores

Authors: Florian Kriebel - *KIT/Karlsruhe Institute of Technology*
Arun Subramaniyan - *KIT/Karlsruhe Institute of Technology*
Semeen Rehman - *KIT/Karlsruhe Institute of Technology*
Segnon Jean Bruno Ahandagbe - *KIT/Karlsruhe Institute of Technology*
Muhammad Shafique - *KIT/Karlsruhe Institute of Technology*
Jörg Henkel - *KIT/Karlsruhe Institute of Technology*

4.1 Improved Hard Real-Time Scheduling of CSDF-modeled Streaming Applications

Authors: Jelena Spasic - *Leiden Univ.*
Di Liu - *Leiden Univ.*
Emanuele Cannella - *Leiden Univ.*
Todor Stefanov - *Leiden Univ.*

EMSOFT

3.1 Numerical Static Analysis of Interrupt-driven Programs via Sequentialization

Authors: Xueguang Wu - *National Univ. of Defense Technology*
Liqian Chen - *National Univ. of Defense Technology*
Antoine Miné - *Centre National de la Recherche Scientifique*
Wei Dong - *National Univ. of Defense Technology*
Ji Wang - *National Univ. of Defense Technology*

3.3 A Scalable Algebraic Method to Infer Quadratic Invariants of Switched Systems

Authors: Xavier Allamigeon - *INRIA & École Polytechnique*
Stephane Gaubert - *INRIA & École Polytechnique*
Eric Goubault - *École Polytechnique*
Sylvie Putot - *École Polytechnique*
Nikolas Stott - *INRIA & École Polytechnique*

4.1 Loosely Time-Triggered Architectures: Improvements and Comparisons

Authors: Guillaume Baudart - *École Normale Supérieure & INRIA*
Albert Benveniste - *INRIA*
Timothy Bourke - *INRIA & École Normale Supérieure*

Sunday, October 4 Schedule

	Lausanne	Winterthur	St. Gallen	Luzern
8:30 - 10:00	**Tutorial 1:** The Beast in Your Memory: Modern Exploitation Techniques and Defenses	**Tutorial 2:** Automating System-Level Design and Modeling Using Meta-Modeling and Code-Generation Techniques	**Tutorial 3:** Unveiling the Foundations and the Practice of Measurement-based Probabilistic Timing Analysis	
10:00 - 10:30	**Coffee (Atrium Foyer)**			
10:30 - 12:00	**Tutorial 1:** The Beast in Your Memory: Modern Exploitation Techniques and Defenses	**Tutorial 2:** Automating System-Level Design and Modeling Using Meta-Modeling and Code-Generation Techniques	**Tutorial 3:** Unveiling the Foundations and the Practice of Measurement-based Probabilistic Timing Analysis	
12:00 - 13:30	**Lunch (Atrium Foyer)**			
13:30 - 15:00	**Tutorial 1:** The Beast in Your Memory: Modern Exploitation Techniques and Defenses	**Tutorial 2:** Automating System-Level Design and Modeling Using Meta-Modeling and Code-Generation Techniques	**Tutorial 4:** Design Challenges in Compute-intensive Mixed-criticality Systems: System, Platform and Application Perspectives	**Tutorial 5:** Parameter-Invariant Monitor Design for Cyber Physical Systems
15:00 - 15:30	**Coffee (Atrium Foyer)**			
15:30 - 17:30	**Tutorial 1:** The Beast in Your Memory: Modern Exploitation Techniques and Defenses	**Tutorial 2:** Automating System-Level Design and Modeling Using Meta-Modeling and Code-Generation Techniques	**Tutorial 4:** Design Challenges in Compute-intensive Mixed-criticality Systems: System, Platform and Application Perspectives	**Tutorial 5:** Parameter-Invariant Monitor Design for Cyber Physical Systems
18:00 - 20:00	**Welcome Reception (Atrium Foyer + Foyer 1)**			

Tutorial 1: The Beast in Your Memory: Modern Exploitation Techniques and Defenses

Time: 8:30 - 17:30 | Room: Lausanne

Memory corruption attacks belong to the most-widely deployed attacks since almost three decades. These attacks have been already applied in the first famous Internet worm (the Morris worm in 1988). Today, they are used to compromise web browsers, launch iOS jailbreaks, and partially in zero day issues exploited in large-scale cyberattacks such as Stuxnet and Duqu. In particular, code-reuse techniques such as return-oriented programming undermine the security model of non-executable memory (the No-Execute Bit) and memory randomization. Defending against these attacks is a hot topic of research. In this tutorial, the attendees will be introduced to the state-of-the-art memory exploitation techniques and defenses. We give an overview of the main principles of memory exploitation covering stack smashing, return-into-libc, and return-oriented programming. We also elaborate on modern defenses such as control-flow integrity and memory randomization. In a hands-on lab, the attendees will construct proof-of-concept exploits targeting mobile platforms (based on ARM).

Speakers:

Ahmed-Reza Sadeghi - *Technische Univ. Darmstadt & Intel Collaborative Research Institute for Secure Computing (ICRI-SC)*
Lucas Davi - *Technische Univ. Darmstadt & Intel Collaborative Research Institute for Secure Computing (ICRI-SC)*

Tutorial 2: Automating System-Level Design and Modeling Using Meta-Modeling and Code-Generation Techniques

Time: 8:30 - 17:30 | Room: Winterthur

The tutorial presents the application of the known software development methodology "Meta-Modeling and Code Generation" to the design of SOCs at system level. Recent research aspects are covered as well as the practical application of the technology. Mainly the semi-automated generation of SystemC virtual prototypes and firmware are covered in the tutorial even if the methodology is able to generate implementation and verification items as well.

Meta-Modeling opens a complete new modeling space for hardware designers. Instead of thinking in models of computation or description languages, the designers think and model in terms of things, attributes of these things and their relationships. The description of involved things, attributes, and relationships is described in a so called Meta-Model. A Model, being an instance of a Meta-Model describes one specific thing with its sub-elements, attribute values and relation settings. The design view, such as a SystemC-TLM model is finally generated from the model.

Speakers:

Wolfgang Ecker - *Infineon Technologies AG*
Rainer Findenig - *Danube Mobile Communications Engineering & Intel Corp.*
Daniel Müller-Gritscheneder - *Technische Univ. München*
Wolfgang Müller - *Univ. of Paderborn & C-Labs LLC*
Munish Jassi - *Technische Univ. München*
Michael Velten - *Infineon Technologies AG*

Tutorial 3: Unveiling the Foundations and the Practice of Measurement-based Probabilistic Timing Analysis

Time: 8:30 - 12:00 | Room: St. Gallen

In the last few years, probabilistic timing analysis (PTA) in general, and its measurement-based variant (MBPTA) in particular, has emergedas a new attractive approach to the problem of the worst-case execution time analysis of software programs.

This tutorial introduces attendees to the foundations and practices of MBPTA and to its relation with the state of the part, with emphasis on what its application exacts from the end user and what it requires from the execution platform. With the help of didactic material and hands-on exercises, participants will be exposed to the whole range of MBPTA concepts and procedures. The tutorial also presents the current advances of MBPTA and the main challenges it has to address to be fully ready for industrial use.

Speakers:

Francisco J. Cazorla - *IIIA-CSIC, Barcelona Supercomputing Center*
Tullio Vardanega - *Univ. of Padua*
Jaume Abella - *Barcelona Supercomputing Center*
Mark Pearce - *Raptita Systems LTD*

Tutorial 4: Design Challenges in Compute-Intensive Mixed-Criticality Systems: System, Platform and Application Perspectives

Time: 13:30 - 17:30 | Room: St. Gallen

Complex embedded systems in domains like automotive and healthcare are evolving into mixed-criticality systems (MCS) in order to meet stringent non-functional requirements relating to cost, quality, safety etc. This tutorial focuses on a class of MCS that involves functionalities requiring compute-intensive processing as well as low-latency time-/safety critical applications (e.g., feedback control loops). Common examples include advanced driver assistance systems (ADAS) in the automotive domain or interventional x-ray (iXR) systems in the healthcare domain. The platforms are migrating from single core to multi-core and, to manycore architectures with various forms of hardware accelerators. At the system-level, an important design decision is the right choice of the platform architecture which further involves translating the application-level requirements into the platform-level requirements. Based on the industrial use-case stemming from the industry-academia collaborations under European Artemis projects EMC2 and ALMARVI, this tutorial will light on: System perspective, Platform perspective and Application perspective.

Speakers:

Teun Hendriks - *TNO, Netherlands*
Zaid Al-Ars - *Delft Univ. of Technology*
Dip Goswami - *Technische Univ. Eindhoven*

Tutorial 5: Parameter-Invariant Monitor Design for Cyber-Physical Systems

Time: 13:30 - 17:30 | Room: Luzern

With recent advances in low-power low-cost communication, sensing, and actuation technologies, Cyber-Physical Systems (CPS) have revolutionized automated medical diagnostics and care, building energy management, and smart grids. With this revolution, dawns a new era of CPS monitoring where fusing measurements from multiple devices provides unprecedented early detection of critical events. However, in some applications (e.g. medical diagnostics) explicit models and/or rich training data relating available measurements to events are unavailable or impractical. Under these troublesome scenarios, this tutorial presents a parameter-invariant approach to monitor design. Owing its mathematical origin to the robust radar signal processing literature, the parameter-invariant approach is presented as consisting of three components: (1) foundations of parameter-invariant design, (2) modeling physical process for monitoring, and (3) constant false alarm rate (CFAR) hypothesis testing. To illustrate each component, this tutorial makes extensive use of case study monitors related to medical alarms, building energy management, and power grids.

Speakers:

James Weimer - *Univ. of Pennsylvania*
Oleg Sokolsky - *Univ. of Pennsylvania*
Insup Lee - *Univ. of Pennsylvania*

Networking Event: Welcome Reception

Time: 18:00 - 20:00 | Room: Atrium Foyer + Foyer 1

All registered ESWeek attendees are cordially invited. All attendees are requested to bring the ESWeek 2015 badges.

Monday, October 5 Schedule

	Matterhorn 2	Matterhorn 1	Matterhorn 3
8:45 - 9:30	**ESWeek Opening Session (Matterhorn 1, 2, & 3)**		
9:30 - 10:30	**Keynote: Enabling the Digital Transformation for a Smarter Life (Matterhorn 1, 2, & 3)** Philippe Magarshack, *STMicroelectronics*		
10:30 - 11:00	**Coffee (Zurich 2, Atrium Foyer & Foyer 1)**		
11:00 - 12:15	Session 1: **CODES + ISSS** - Novel Memory Architecture and Memory Management	Session 1: **EMSOFT** - Real-Time Systems	Session 1: **CASES** - Power and Energy
12:15 - 12:45	**Poster (Atrium Foyer + Zurich 2)**		
12:45 - 14:15	**Lunch (Zurich 2, Atrium Foyer & Foyer 1)**		
14:15 - 15:30	Special Session 2: **CODES + ISSS** - Design Methodologies for Securing Cyber-Physical Systems	Special Session 2: **EMSOFT** - Verification and Analysis of Hybrid Systems	Special Session 2: **CASES** - Computing at the Margins in Embedded Systems
15:30 - 16:00	**Poster with coffee (Zurich 2, Atrium Foyer & Foyer 1)**		
16:00 - 17:15	Session 3: **CODES + ISSS** - Software Technologies for Mobile and Real-Time Embedded Systems	Session 3: **EMSOFT** - Abstract Interpretation	Session 3: **CASES** - System Reliability
17:15 - 17:45	**Poster (Atrium Foyer + Zurich 2)**		
17:45 - 18:15	**SIGBED Meeting**		

Keynote: Enabling the Digital Transformation for a Smarter Life

Philippe Magarshack - *Executive Vice President, CTO, Embedded Processing Solutions, STMicroelectronics*

Time: 9:30 - 10:30 | Room: Matterhorn 1, 2, & 3

The digital transformation is accelerating disruptions in all industries and areas of human activity. As the world around us becomes smarter and more connected all aspects of the way we conduct business and our daily lives are impacted with constantly evolving new services through the Internet of Things. This revolution is both a great opportunity and a significant challenge for the broad electronics industry and in particular for the semiconductor industry. We will describe the opportunities and the challenges of this radical transformation, and we will provide our vision on some of the evolutions that are needed to succeed in this transformation.

Biography

From 1985 to 1989, Magarshack worked as a microprocessor designer at AT&T Bell Labs in the USA. In 1989, he joined Thomson-CSF in Grenoble, France, and took responsibility for libraries and ASIC design kits for the military market. In 1994, Magarshack joined the Central R&D Group of SGS-THOMSON Microelectronics (now STMicroelectronics), where he held several roles in CAD and Libraries management for advanced integrated-circuit manufacturing processes. In 2005, Magarshack was appointed Group Vice President and General Manager of Central CAD and Design Solutions at STMicroelectronics' Technology R&D and Manufacturing organization. In 2012, he was promoted to ST's Executive Vice President in charge of Design Enablement & Services.

Magarshack has been President of the Minalogic Collaborative R&D Cluster in Grenoble since June 2014.

Philippe Magarshack graduated from Ecole Polytechnique, Palaiseau, France, and holds an Electronics Engineering degree from Ecole Nationale Supérieure des Télécommunications in Paris, France.

Session 1: CASES - Power and Energy

Time: 11:00 - 12:15 | Room: Matterhorn 3

Chairs:

Aviral Shrivastava - *Arizona State Univ.*
Muhammad Al-Faruque - *University of California Irvine*

1.1 Embedded System and Application Aware Design of Deregulated Energy Delivery Systems
Xuejing He, **Robert P. Dick** - *Univ. of Michigan*
Russ Joseph - *Northwestern Univ.*

1.2 Optimizing Mobile Display Brightness by Leveraging Human Visual Perception
Matthew Schuchhardt - *Northwestern Univ,*
Susmit Jha, Raid Ayoub, Michael Kishinevsky - *Intel Corp.*
Gokhan Memik - *Northwestern Univ.*

1.3 QuadSeal: Quadruple Algorithmic Symmetrizing Countermeasure Against Power Based Side-channel Attacks
Darshana Jayasinghe, Aleksandar Ignjatovic - *Univ. of New South Wales*
Jude Angelo Ambrose - *Canon Information Systems Research Australia Pty. Ltd.*
Roshan Ragel - *Univ. of Peradeniy*
Sri Parameswaran - *Univ. of New South Wales*

Session 1: CODES + ISSS - Novel Memory Architecture and Memory Management

Time: 11:00 - 12:15 | Room: Matterhorn 2

Chairs:

Kim Grüttner - *OFFIS – Institute for Information Technology*
Christian Haubelt - *Univ. of Rostock*

1.1 R2Cache: Reliability-Aware Reconfigurable Last-Level Cache Architecture for Multi-Cores
Florian Kriebel, Arun Subramaniyan, Semeen Rehman,
Segnon Jean Bruno Ahandagbe, Muhammad Shafique,
Jörg Henkel - *KIT/Karlsruhe Institute of Technology*

1.2 How to Improve the Space Utilization of Dedup-based PCM Storage Devices?
Chun-Ta Lin - *National Taiwan Univ.*
Yuan-Hao Chang - *Academia Sinica*
Tei-Wei Kuo - *Academia Sinica and National Taiwan Univ.*
Hung-Sheng Chang - *National Taiwan Univ.*
Hsiang-Pang Li - *Macronix International Co., Ltd.*

1.3 A Tiny-Capacitor-backed Non-volatile Buffer to Reduce Storage Writes in Smartphones
Mungyu Son - *Pohang Univ. of Science and Technology*
Junwhan Ahn, Sungjoo Yoo - *Seoul National Univ.*

Session 1: EMSOFT - Real-Time Systems

Time: 11:00 - 12:15 | Room: Matterhorn 1

Chairs:

Marc Pouzet - *Ecole Normale Supérieure*
Jian-Jia Chen - *TU Dortmund*

1.1 The Federated Scheduling of Systems of Conditional Sporadic DAG Tasks
Sanjoy Baruah - *Univ. of North Carolina, Chapel Hill*

1.2 Adaptive Runtime Shaping for Mixed-Criticality Systems
Biao Hu, Kai Huang, Gang Chen, Long Cheng,
Alois Knoll - *Technische Univ. München*

1.3 Can Real-Time Systems be Chaotic?
Lothar Thiele - *Eidgenössische Technische Hochschule Zürich*
Pratyush Kumar - *Swiss Federal Institute of Technology*

Special Session 2: CASES - Computing at the Margins in Embedded Systems

Time: 14:15 - 15:30 | Room: Matterhorn 3

Chair:

Hadi Esmaeilzadeh - *Georgia Institute of Technology*

Organizers:

Hadi Esmaeilzadeh - *Georgia Institute of Technology*
John Augustine - *Indian Institute of Technology Madras*

2.1 Approximate Acceleration: A Path through the Era of Dark Silicon and Big Data
Hadi Esmaeilzadeh - *Georgia Institute of Technology*

2.2 Does Customizing Inexactness Help Over Simplistic Precision (bit-width) Reduction? A Case Study
Ashutosh Ingole, Biswaroop Maiti,
John Augustine - *Indian Institute of Technology Madras*
Krishna Palem - *Rice Univ.*

2.3 Energy-interference-free System and Toolchain Support for Energy-harvesting Devices
Alexei Colin - *Carnegie Mellon Univ.*
Alanson P. Sample - *Disney Research, Pittsburgh*
Brandon Lucia - *Carnegie Mellon Univ.*

2.4 Accuracy-Aware Optimization of Approximate Programs
Sasa Misailovic - *Massachusetts Institute of Technology*

Special Session 2: CODES + ISSS - Design Methodologies for Securing Cyber-Physical Systems

Time: 14:15 - 15:30 | Room: Matterhorn 2

Chair:
Miroslav Pajic - *Duke Univ.*

Organizer:
Mohammad Abdullah Al Faruque - *Univ. of California, Irvine*

Security has been seen as one of the major design challenges for CPS both in academia and industry. Standard design techniques used for securing embedded systems are not suitable for CPS, due to the restrict computation and communication budget available in the latter. To address these issues, it is required a novel design approach in which security is considered since the beginning of the whole design flow and addressed in a holistic way. This special session addresses the issues related with design of secure CPS.

The first talk will discuss about the multi-disciplinary modeling, simulation, tools, and software synthesis challenges for CPS. The second presentation will highlight a novel framework to design secured control system for the CPS, while taking into account properties of the underlying computation and communication platform.
Finally, the third talk will present the security challenges in the computing hardware within the CPSs.

2.1 Design for Security: Modeling and Design Automation Tools for Cyber-Physical Systems Security
Mohammad Al Faruque - *Univ. of California, Irvine*

2.2 Platform-Aware Design Framework for Securing Cyber-Physical Systems
Miroslav Pajic - *Duke Univ.*

2.3 The Hardware Side of Security for Cyber-Physical Systems
Francesco Regazzoni - *ALaRI*

Special Session 2: EMSOFT - Verification and Analysis of Hybrid Systems

Time: 14:15 - 15:30 | Room: Matterhorn 1

Chairs:
Lothar Thiele - *ETHZ*
Truong X. Nghiem - *EPFL*

2.1 Requirements Driven Falsification with Coverage Metrics
Georgios Fainekos, Adel Dokhanchi - *Arizona State Univ.*
Aditya Zutshi - *Univ. of Colorado*
Rahul T. Sriniva - *Arizona State Univ.*
Sriram Sankaranarayanan - *Univ. of Colorado*

2.2 Reachability of Hybrid Systems in Space-Time
Goran Frehse - *Univ. Grenoble Alpes*

2.3 Unbounded-Time Reachability Analysis of Hybrid Systems by Abstract Acceleration
Peter Schrammel - *Univ. of Oxford*

Session 3: CASES - System Reliability

Time: 16:00 - 17:15 | Room: Matterhorn 3

Chairs:

Henri-Pierre Charles - *CEA*
Muhammad Shafique - *Karlsruhe Institute of Technology*

3.1 Evaluating and Exploiting Impacts of Dynamic Power Management Schemes on System Reliability
Liangzhen Lai - *Univ. of California, Los Angeles*
Vikas Chandra - *ARM, Inc.*
Puneet Gupta - *Univ. of California, Los Angeles*

3.2 Exploiting Cache Conflicts to Reduce Radiation Sensitivity of Operating Systems on Embedded Systems
Thiago Santini, **Paolo Rech**, Luigi Carro,
Flavio Rech Wagner - *Univ. Federal do Rio Grande do Sul*

3.3 Optimization of Multi-Channel BCH Error Decoding for Common Cases
Russ Dill, Aviral Shrivastava - *Arizona State Univ.*
Hyunok Oh - *Hanyang Univ.*

Session 3: CODES + ISSS - Software Technologies for Mobile and Real-Time Embedded Systems

Time: 16:00 - 17:15 | Room: Matterhorn 2

Chairs:

Steffen Peter - *Univ. of California, Irvine*
Peter Marwedel - *Technische Univ. Dortmund*

3.1 LearnLoc: A Framework for Smart Indoor Localization with Embedded Mobile Devices
Sudeep Pasricha - *Colorado State Univ.*
Viney Ugave - *IBM Corp.*
Qi Han - *Colorado School of Mines*
Chuck Anderson - *Colorado State Univ.*

3.2 Lightweight Virtual Memory Support for Many-Core Accelerators in Heterogeneous Embedded SoCs
Pirmin Vogel, Andrea Marongiu,
Luca Benini - *Eidgenössische Technische Hochschule Zürich*

3.3 Analysis and Optimization of Soft Error Tolerance Strategies for Real-time Systems
Bowen Zheng - *Univ. of California, Riverside*
Yue Gao - *Univ. of Southern California*
Qi Zhu - *Univ. of California, Riverside*
Sandeep Gupta - *Univ. of Southern California*

Session 3: EMSOFT - Abstract Interpretation

Time: 16:00 - 17:15 | Room: Matterhorn 1

Chairs:

Alain Girault - *INRIA*
Florence Maraninchi - *Univ. Grenoble Alpes, Verimag, France*

3.1 Numerical Static Analysis of Interrupt-driven Programs via Sequentialization
Xueguang Wu, Liqian Chen - *National Univ. of Defense Technology*
Antoine Miné - *Centre National de la Recherche Scientifique*
Wei Dong, Ji Wang - *National Univ. of Defense Technology*

3.2 Towards an Industrial Use of Sound Static Analysis for the Verification of Concurrent Embedded Avionics Software
Antoine Miné - *Centre National de la Recherche Scientifique*
David Delmas - *Airbus S.A.S.*

3.3 A Scalable Algebraic Method to Infer Quadratic Invariants of Switched Systems
Xavier Allamigeon, Stephane Gaubert - *INRIA*
Eric Goubault, Sylvie Putot - *École Polytechnique*
Nikolas Stott - *INRIA*

Tuesday, October 6 Schedule

	Matterhorn 2	Matterhorn 1	Matterhorn 3
8:30 - 9:30	**Keynote: Evolution or Revolution? Requirements for the Architecture of Automated Vehicles (Matterhorn 1, 2, & 3)** Michael Fausten, *Robert Bosch GmbH*		
9:30 - 10:30	**Keynote: Fast Model Predictive Control (Matterhorn 1, 2, & 3)** Manfred Morari, *Swiss Federal Institute of Technology*		
10:30 - 11:00	**Coffee (Zurich 2, Atrium Foyer & Foyer 1)**		
11:00 - 12:15	Session 4: **CODES + ISSS** - Advanced Design Methodologies	Session 4: **EMSOFT** - Synchronous Programming and Dataflow Systems	Session 4: **CASES** - Approximate Computing
12:15 - 12:45	**Poster (Atrium Foyer + Zurich 2)**		
12:45 - 14:15	**Lunch (Zurich 2, Atrium Foyer & Foyer 1)**		
14:15 - 15:30	Special Session 5: **CODES + ISSS** - Power-Awareness and Smart-Resource Management in Embedded Computing Systems	Special Session 5: **EMSOFT** - Design of Hybrid Systems	Session 5: **CASES** - Vector Processing
15:30 - 16:00	**Poster with coffee (Zurich 2, Atrium Foyer & Foyer 1)**		
16:00 - 17:15	Session 6: **CODES + ISSS** - System Trade-Offs and Monitoring: Performance, Energy, Temperature, and Ageing	Session 6: **EMSOFT** - Energy Efficiency and Security	Session 6: **CASES** - Multi-Core Architectures
17:15 - 17:30	**Poster (Atrium Foyer + Zurich 2)**		
18:00 - 22:30	**Networking Event: Amsterdam Canals Boat Tour and Conference Banquet Gala**		

Keynote: Evolution or Revolution? Requirements for the Architecture of Automated Vehicles

Michael Fausten - *VP Vehicle Systems Development, Robert Bosch GmbH*

Time: 8:30 - 9:30 | Room: Matterhorn 1, 2 & 3

Highly automated driving has become a major trend in automotive industry. As a system supplier Bosch is investigating the system impacts, that automated driving has on the major subsystems and components, such as sensors, braking and steering systems, control units, in-vehicle communication, connectivity and many more.

Automated driving brings three major challenges:
1) High performance: Algorithms for automated driving are challenging with respect to calculation power, memory and communication. They thus require high performance electronic components.

2) High reliability: Since highly automated vehicles take full responsibility for the vehicle's behavior, the complete system needs to be highly reliable and imposes high challenges on safety. Furthermore, the automated driving system and thus its electronic components need to perform safely even in backup and failure mode.

3) Connectivity and Security: Automated vehicles will be connected. Connected vehicles need to be protected against any security threats in order to guarantee safe operation and privacy of data. Electronic components need to be prepared for high level security.

The presented paper derives impacts on the vehicle's electronics, starting from the high level system requirements of automated driving.

Biography

Michael Fausten became project manager for automated driving in 2011. Since 2013, he has also held the post of vice president vehicle systems development in the Chassis Systems Control division at Robert Bosch GmbH in Abstatt.

Michael Fausten was born in Cologne, Germany, in 1969. After passing his university entrance examination, he studied physics at the University of Bonn. Following his undergraduate studies, he earned a PhD in electrical engineering at the Technische Universität Berlin. Fausten joined Robert Bosch GmbH in 1997, starting at the company's Toluca location in Mexico. Since 2001, he has held a variety of positions in the development and pre-development of connected chassis systems, which has included work on vehicle dynamics management and combined active and passive safety.

Keynote: Fast Model Predictive Control

Manfred Morari - *Swiss Federal Institute of Technology*

Time: 9:30 - 10:30 | Room: Matterhorn 1, 2 & 3

In the 1980s Model Predictive Control (MPC) became the algorithm of choice in the process industries for demanding multi-variable applications involving constraints. Today's vastly more powerful computational resources and a series of new algorithms have made these tools suitable for problems of essentially any size and time scale. I will describe the road taken and illustrate the effectiveness with industrial examples from the automotive and power electronics domains and the industrial energy sector. In the final part of the lecture I will suggest topics of future research.

Biography

Manfred Morari was head of the Department of Information Technology and Electrical Engineering at ETH Zurich from 2009 to 2012. He was head of the Automatic Control Laboratory from 1994 to 2008. Before that he was the McCollum-Corcoran Professor of Chemical Engineering and Executive Officer for Control and Dynamical Systems at the California Institute of Technology. He obtained the diploma from ETH Zurich and the Ph.D. from the University of Minnesota, both in chemical engineering. His interests are in hybrid systems and the control of biomedical systems.

Morari's research is internationally recognized. The analysis techniques and software developed in his group are used in universities and industry throughout the world. He has received numerous awards, including the Eckman Award, Ragazzini Award and Bellman Control Heritage Award from the American Automatic Control Council; the Colburn Award, Professional Progress Award and CAST Division Award from the American Institute of Chemical Engineers (AIChE); the Nyqvist Lectureship and the Oldenburger Medal of the American Society of Mechanical Engineering, the Control Systems Award and the Bode Lecture Prize from IEEE. He is a Fellow of IEEE, AIChE and IFAC. In 1993 he was elected to the U.S. National Academy of Engineering.

Session 4: CASES - Approximate Computing

Time: 11:00 - 12:15 | Room: Matterhorn 3

Chairs:

Akash Kumar - *National Univ. of Singapore*
Brandon Lucia - *Carnegie Mellon University*

4.1 Program Analysis for Approximation-aware Compilation
Pooja Roy, Jianxing Wang, Weng Fai Wong - *National Univ. of Singapore*

4.2 Approximation-Aware Multi-Level Cells STT-RAM Cache Architecture
Felipe Sampaio - *Univ. Federal do Rio Grande do Sul*
Muhammad Shafique - *KIT/Karlsruhe Institute of Technology*
Bruno Zatt - *Univ. Federal de Pelotas*
Sergio Bampi - *Univ. Federal do Rio Grande do Sul*
Jörg Henkel - *KIT/Karlsruhe Institute of Technology*

4.3 Quality-Aware Data Allocation in Approximate DRAM
Arnab Raha, Hrishikesh Jayakumar, Soubhagya Sutar,
Vijay Raghunathan - *Purdue Univ.*

Session 4: CODES + ISSS - Advanced Design Methodologies

Time: 11:00 - 12:15 | Room: Matterhorn 2

Chairs:

Sungjoo Yoo - *Seoul National Univ.*
Sudeep Pasricha - *Colorado State Univ.*

4.1 Improved Hard Real-Time Scheduling of CSDF-modeled Streaming Applications
Jelena Spasic, Di Liu, Emanuele Cannella, Todor Stefanov - *Leiden Univ.*

4.2 DsReliM: Power-Constrained Reliability Management in Dark-Silicon Many-Core Chips under Process Variations
Mohammad Salehi, **Muhammad Shafique**, Florian Kriebel,
Semeen Rehman - *KIT/Karlsruhe Institute of Technology*
Mohammad Khavari Tavana - *George Mason Univ.*
Alireza Ejlali - *Sharif Univ. of Technology*
Jörg Henkel - *KIT/Karlsruhe Institute of Technology*

4.3 Hardware Synthesis from a Recursive Functional Language
Kuangya Zhai, Richard Townsend, Lianne Lairmore, Martha Kim,
Stephen Edwards - *Columbia Univ.*

Session 4: EMSOFT - Synchronous Programming and Dataflow Systems

Time: 11:00 - 12:15 | Room: Matterhorn 1

Chairs:

Miroslav Pajic - *Univ. of Pennsylvania*
Weichen Liu - *Chongqing Univesity*

4.1 Loosely Time-Triggered Architectures: Improvements and Comparisons
Guillaume Baudart - *École normale supérieure & INRIA*
Albert Benveniste - *INRIA*
Timothy Bourke - *INRIA*

4.2 Parametrized Dataflow Scenarios
Mladen Skelin - *Norwegian Univ. of Science and Technology*
Marc Geilen - *Eindhoven Univ. of Technology*
Francky Catthoor - *IMEC*
Sverre Hendseth - *Norwegian Univ. of Science and Technology*

4.3 Executing Dataflow Actors as Kahn Processes
Andreas Tretter - *Eidgenössische Technische Hochschule Zürich*
Jani Boutellier - *Univ. of Oulu*
James Guthrie, Lars Schor, Lothar Thiele
- *Eidgenössische Technische Hochschule Zürich*

Session 5: CASES - Vector Processing

Time: 14:15 - 15:30 | Room: Matterhorn 3

Chairs:

Heiko Falk - *Technical Univ. of Hamburg*
Puneet Gupta - *Univ. of California, Los Angeles*

5.1 Vector-Aware Register Allocation for GPU Shader Processors
Yi-Ping You, Szu-Chieh Chen - *National Chiao Tung Univ.*

5.2 A Sparse Matrix Vector Multiply Accelerator for Support Vector Machine
Eriko Nurvitadhi, Asit Mishra, Debbie Marr - *Intel Corp.*

5.3 Saving Memory Movements Through Vector Processing in the DRAM
Marco Antonio Zanata Alves, Paulo Santos, Francis Birck Moreira, Matthias Diener, **Luigi Carro** - *Univ. Federal do Rio Grande do Sul*

Special Session 5: CODES + ISSS - Power-Awareness and Smart-Resource Management in Embedded Computing Systems

Time: 14:15 - 15:30 | Room: Matterhorn 2

Organizer:

Donatella Sciuto - *Politecnico di Milano*

Multicore processors have become prevalent in the whole spectrum of computing systems, ranging from embedded solutions like mobile handheld devices Computer architectures can leverage reconfigurable fabrics to dynamically support the performance/power requirements of fluctuating loads; compilers and runtimes can automatically tune code generation to better exploit the underlying computer architecture to reach the sweet-spot in terms of performance per Watt; operating systems can implement smart resource management techniques leveraging the dynamic knobs provided by both computer architectures and compilers.

5.1 The HELIX Parallelizing Compiler to Efficiently Manage Resources
Simone Campanoni - *Harvard Univ.*

5.2 Operating System-Level Performance and Power Management: from Datacenters to Embedded Systems
Marco D. Samtambrogio, Alessandro Antonio Nacci, Gianluca Carlo Durelli, Matteo Ferroni, Riccardo Cattaneo - *Politecnico di Milano*

5.3 Power-Transmission and Work-Balancing Policies in the e-Health Mobile Cloud Computing Scenario
Josue Pagan, Marina Zapater - *Complutense Univ. of Madrid*
Monica Vallejo - *Columbia Univ.*
Jose L. Ayala - *Complutense Univ. of Madrid*

Special Session 5: EMSOFT - Design of Hybrid Systems

Time: 14:15 - 15:30 | Room: Matterhorn 1

Chairs:

Goran Frehse - *Univ. Grenoble Alpes*
Marc Geilen - *Eindhoven University of Technology*

5.1 Modeling and Simulating Cyber-Physical Systems Using CyPhySim
Edward A. Lee, Mehrdad Niknami - *Univ. of California, Berkeley*
Thierry S. Nouidui, Michael Wetter - *Lawrence Berkeley National Lab*

5.2 Building a Hybrid Systems Modeler from Synchronous Language Principles
Marc Pouzet - *École Normale Supérieure, Paris*

5.3 Formal Verification of ACAS X, an Industrial Airborne Collision Avoidance System
Jean-Baptiste Jeannin, Khalil Ghorbal - *Carnegie Mellon Univ.*
Yanni Kouskoulas, Ryan Gardner, Aurora Schmidt - *Johns Hopkins Univ.*
Erik Zawadzki, André Platzer - *Carnegie Mellon Univ.*

Session 6: CASES - Multi-Core Architectures

Time: 16:00 - 17:15 | Room: Matterhorn 3

Chairs:

Oliver Bringmann - *Univ. Tübingen*
Sudeep Pasricha - *Colorado State University*

6.1 Efficient SAT-based Application Mapping and Scheduling on Multiprocessor Systems for Throughput Maximization
Weichen Liu - *Chongqing Univ.*
Zonghua Gu - *Zhejiang Univ.*
Yaoyao Ye - *Shanghai Jiao Tong Univ.*

6.2 NUVA: Architectural Support for Runtime Verification of Parametric Specifications over Multicores
Ahmed Nassar, **Fadi Kurdahi,** Wael Elsharkasy - *Univ. of California, Irvine*

6.3 High Performance and Energy Efficient Wireless NoC-Enabled Multicore Architecture for Graph Analytics
Karthi Duraisamy, Hao Lu, **Partha Pande**,
Ananth Kalyanaraman - *Washington State Univ.*

Session 6: CODES + ISSS - System Trade-Offs and Monitoring: Performance, Energy, Temperature, and Ageing

Time: 16:00 - 17:15 | Room: Matterhorn 2

Chairs:

Frédéric Rousseau - *TIMA Lab, CNRS/Grenoble INP/UJF*
Preeti Ranjan Panda - *Indian Institute of Technology, Delhi*

6.1 SeBoost: Selective Boosting for Heterogeneous Manycores
Santiago Pagani, Muhammad Shafique,
Heba Khdr - *KIT/Karlsruhe Institute of Technology*
Jian-Jia Chen - *Technische Univ. Dortmund*
Jörg Henkel - *KIT/Karlsruhe Institute of Technology*

6.2 An Online Wear State Monitoring Methodology for Off-the-Shelf Embedded Processors
Srinath Arunachalam, Thidapat Chantem - *Utah State Univ.*
Robert P. Dick - *Univ. of Michigan*
Xiaobo Sharon Hu - *Univ. of Notre Dame*

6.3 Big/Little Deep Neural Network for Ultra Low Power Inference
Eunhyeok Park - *Seoul National Univ.*
Dongyoung Kim - *Pohang Univ. of Science and Technology*
Soobeom Kim - *Seoul National Univ.*
Yougdeok Kim - *Samsung Electronics Co., Ltd.*
Sungroh Yoon, Gunhee Kim, Sungjoo Yoo - *Seoul National Univ.*

Session 6 - EMSOFT - Energy Efficiency and Security

Time: 16:00 - 17:15 | Room: Matterhorn 1

Chairs:

Sanjoy Baruah - *Univ. of North Carolina*
Renato Mancuso - *Univ. of Illinois at Urbana-Champaign*

6.1 Scalable Scheduling of Energy Control Systems
Truong Nghiem - *École Polytechniquecole Polytechnique Fédérale de Lausanne*
Rahul Mangharam - *Univ. of Pennsylvania*

6.2 Distributed Power Management of Real-time Applications on a GALS Multiprocessor SOC
Andrew Nelson, Kees Goossens - *Technische Univ. Eindhoven*

6.3 Exp-HE: A Family of Fast Exponentiation Algorithms Resistant to SPA, Fault, and Combined Attacks
Carlos Moreno, M. Anwar Hasan, Sebastian Fischmeister - *Univ. of Waterloo*

Networking Event: Amsterdam Canals Boat Tour and Conference Banquet Gala

Time: 18:00 - 22:30

Boat Tour

Time
17:30 – 18:00 Boarding on the boats
18:00 – 19:00 Boat tour
19:00 Boat tour ends and attendees are dropped off at the Banquet location (Westerkerk)

Location
The meeting point to board the boats and other relevant information will be provided at the ESWeek 2015 opening session.

Remarks
All registered ESWeek attendees are cordially invited. All attendees are requested to bring the ESWeek 2015 badges.

Conference Banquet Gala

Time: 19:00 – 22:30

Location
Westerkerk Amsterdam, Prinsengracht 281, 1016 GW AMSTERDAM

Remarks
All registered ESWeek attendees are cordially invited. All attendees are requested to bring the ESWeek 2015 badges. Extra banquet coupons (for family members, etc.) could be purchased at the ESWeek Registration and Information Desk.

Wednesday, October 7 Schedule

	Matterhorn 2	Matterhorn 1	Matterhorn 3	Zurich 1
8:30 - 9:30	**Keynote: Connected Vehicles - Cars Talking to Each Other, Safe & Securely (Matterhorn 1, 2, & 3)** Mark Steigemann, *NXP Semiconductors*			
9:30 - 10:45	Session 7: **CODES + ISSS** - Domain-Specific Systems			Session 7: **EMSOFT** - Data Mining
10:45 - 11:15	**Coffee (Zurich 2, Atrium Foyer & Foyer 1)**			
11:15 - 12:30	Session 8A: **CODES + ISSS** - Hardware/Software Solutions for the Design and Optimization of Networked Embedded Systems	Session 8: **EMSOFT** - Memory Management	Session 7: **CASES** - Scheduling, Timing and Locality	Session 8B: **CODES + ISSS** - Accelerating System Verification
12:30 - 13:00	**Poster: First and Second Session (Atrium Foyer + Zurich 2)**			
13:00 - 14:15	**Lunch (Zurich 2, Atrium Foyer & Foyer 1)**			
14:15 - 15:30	Special Session 9: **CODES + ISSS** - The Shift to Multicores in Real-Time and Safety-Critical Systems	Session 9A: **EMSOFT** - Formal Verification	Special Session 8: **CASES** - Wearable Self-Powered Systems	Session 9B: **EMSOFT** - Networked Systems
15:30 - 16:00	**Poster with Coffee (Zurich 2, Atrium Foyer & Foyer 1)**			
16:00 - 17:30	**Panel: Embedded System Security - What Does It Change?** **Moderator:** Sri Parameswaran **Panelists:** Georg Sigl - *Technische Univ. München*, Mark Steigemann - *NXP Semiconductors*, Nathalie Feyt - *Thales,* Oleg Sokolsky - *Univ. of Pennsylvania*			

Keynote: Connected Vehicles - Cars Talking to Each Other, Safe & Securely

Mark Steigemann - *Senior Director Product Architecture, Business Unit Automotive, NXP Semiconductors*

Time: 8:30 - 9:30 | Room: Matterhorn 1, 2 & 3

Hyper-connectivity is changing our world, forever!
With more than 50 Billion devices being connected by 2020, safe and secure connections will be one of the many key challenges we have to master.

There are a number of key trends causing a paradigm shift in automotive electronics industry, since a few years. Energy efficiency, automated cars, seamless user experience. The content of electronic units in the car is growing rapidly to support us in our daily live. Cars are getting more secure, more energy efficient, more autonomous, and they connect to each other and the cloud.

This talk will introduce the audience to recent developments in automotive electronics such as Car2 Car communication, Driver assistance systems and intelligent networking, and why cars need to be connected to the IoT space and amongst each other. Observing the problems from different perspectives (car, driver, authorities), the talk will put light on Car level security to protect content and identities, hacking prevention and the aspects of a secure ecosystem.

Biography

Mark Steigemann currently holds the position of a Senior Director & Chief Architect in the Automotive group of NXP Semiconductors. In this capacity he is responsible for product architecture definition and strategic roadmap planning in the Car Infotainment and Driver assistance division. Mark has a strong track record in bringing innovations to products. He joined NXP (formerly Philips Semiconductors) in 1998, has since then held key leadership positions in various technical domains. Since 2005 he is working as Technology Manager & Lead Architect in Automotive Business unit, where his main responsibility include product architecture definition for worldwide digital radio systems, coordination of research and technology programs required for product development. Since 2013, he is heading the Product architecture group in the Infotainment and Driver assistance division. With his team of senior technical experts he is coordinating long term Product roadmap definition on System level, partitioning strategies, company-wide platform architecture definition, IP/Technology portfolio definition for the RFCMOS Radar, Car2Car and Infotainment domain.

Session 7 - CODES + ISSS - Domain-Specific Systems

Time: 9:30 - 10:45 | Room: Matterhorn 2

Chairs:

Roberta Piscitelli - *TNO, Netherlands*
Mohammad Abdullah Al Faruque - *Univ. of California, Irvine*

7.1 An Approximate Compressor for Wearable Biomedical Healthcare Monitoring Systems
Farzad Samie, Lars Bauer, Jörg Henkel - *KIT/Karlsruhe Institute of Technology*

7.2 Computer Security by Hardware-Intrinsic Authentication
Caio Hoffman, Mario Cortes, Diego F. Aranha, Guido Araujo - *Univ. of Campinas*

7.3 Energy Efficient FFT Implementation through Stage Skipping and Merging
Namita Sharma, **Preeti Ranjan Panda** - *Indian Institute of Technology, Delhi*
Francky Catthoor - *IMEC*

Session 7 - EMSOFT - Data Mining

Time: 9:30 - 10:45 | Room: Zurich 1

Chairs:

Oleg Sokolsky - *Univ. of Pennsylvania*
Wang Yi - *Uppsala University*

7.1 Data Mining Approach to Temporal Debugging of Embedded Streaming Applications
Oleg Iegorov - *Univ. Grenoble Alpes - CEA, LETI*
Alexandre Termier - *Univ. of Rennes 1*
Vincent Leroy, Jean-François Méhaut - *Univ. Grenoble Alpes - CEA, LETI*
Miguel Santana - *STMicroelectronics*

7.2 A Framework for Mining Hybrid Automata from Input/Output Traces
Ramy Medhat - *Univ. of Waterloo*
Ramesh S. - *General Motors Research and Development*
Borzoo Bonakdarpour, Sebastian Fischmeister - *Univ. of Waterloo*

Session 7: CASES - Scheduling, Timing and Locality

Time: 11:15 - 12:30 | Room: Matterhorn 3

Chairs:

Sebastian Fischmeister - *Univ. of Waterloo*
Jingtong Hu - *Oklahoma State University*

7.1 Timing Characterization of OpenMP4 Tasking Model
Maria A. Serrano - *Barcelona Supercomputing Center*
Alessandra Melani - *Scuola Superiore Sant'Anna*
Roberto Vargas - *Barcelona Supercomputing Center*
Andrea Marongiu - *Eidgenössische Technische Hochschule Zürich*
Marko Bertogna - *Univ. of Modena and Reggio Emilia*
Eduardo Quinones - *Barcelona Supercomputing Center*

7.2 Scheduling Instruction Effects for a Statically Pipelined Processor
Brandon Davis, Peter Gavin, Ryan Baird - *Florida State Univ.*
Magnus Sjalander - *Uppsala Univ.*
Ian Finlayson, - *Univ. of Mary Washington*
Farhad Rasapour, Gregory Cook - *Boise State Univ.*
Gang-Ryung Uh, David Whalley, Gary Tyson - *Florida State Univ.*

7.3 Reducing Shift Penalty in Domain Wall Memory through Register Locality
Ehsan Atoofian - *Lakehead Univ.*

Session 8A: CODES + ISSS - Hardware/Software Solutions for the Design and Optimization of Networked Embedded Systems

Time: 11:15 - 12:30 | Room: Matterhorn 2

Chairs:

Sander Stuijk - *Technische Univ. Eindhoven*
Muhammad Shafique - *KIT/Karlsruhe Institute of Technology*

8A.1 Fast Parallel Application and Multiprocessor Design Space Exploration from Sequential Code
Vítor Schwambach, Sébastien Cleyet-Merle, Alain Issard - *STMicroelectronics*
Stéphane Mancini - *TIMA Lab, CNRS/Grenoble INP/UJF*

8A.2 Run-DMC: Runtime Dynamic Heterogeneous MultiCore Performance and Power Estimation for Energy Efficiency
Tiago Muck, Santanu Sarma, Nikil Dutt - *Univ. of California, Irvine*

8A.3 Transparent and Portable Agent Based Task Migration for Data-Flow Applications on Multi-Tiled Architectures
Ashraf Elantably, Olivier Gruber, Nicolas Fournel,
Frédéric Rousseau - *Univ. Grenoble Alpes*

Session 8B: CODES + ISSS - Accelerating System Verification

Time: 11:15 - 12:30 | Room: Zurich 1

Chairs:

Gero Dittmann - *IBM Research - Zurich*
Martin Radetzki - *Univ. of Stuttgart*

8B.1 A Parallelizable Approach for Mining Likely Invariants
Graziano Pravadelli, **Alessandro Danese**, Luca Piccolboni - *Univ. of Verona*

8B.2 Completeness Bounds and Sequentialization for Model Checking of Interacting Firmware and Hardware
Sunha Ahn, Sharad Malik, Aarti Gupta - *Princeton Univ.*

8B.3 Fault Injection Acceleration by Architectural Importance Sampling
Mojtaba Ebrahimi, Nour Sayed, Maryam Rashvand
Mehdi Tahoori - *KIT/Karlsruhe Institute of Technology*

Session 8: EMSOFT - Memory Management

Time: 11:15 - 12:30 | Room: Matterhorn 1

Chairs:

Aviral Shrivastava - *Arizona State Univ.*
Jason Xue - *City University of Hong Kong*

8.1 Static Memory Management for Efficient Mobile Sensing Applications
Farley Lai, Daniel Schmidt, **Octav Chipara** - *Univ. of Iowa*

8.2 Nonvolatile Main Memory Aware Garbage Collection in High-Level Language Virtual Machine
Chen Pan, Mimi Xie - *Oklahoma State Univ.*
Chengmo Yang - *Univ. of Delaware*
Zili Shao - *Hong Kong Polytechnic Univ.*
Jingtong Hu - *Oklahoma State Univ.*

8.3 Managing GPU Buffers for Caching More Apps in Mobile Systems
Sejun Kwon - *Sungkyunkwan Univ.*
Sang-Hoon Kim - *Korea Advanced Institute of Science and Technology*
Jin-Soo Kim, Jinkyu Jeong - *Sungkyunkwan Univ.*

Special Session 8: CASES - Wearable Self-Powered Systems

Time: 14:15 - 15:30 | Room: Matterhorn 3

Chair:

Jason Xue - *City Univ. of Hong Kong*

8.1 Self-Powered Wearable Sensor Platforms for Wellness

Veena Misra - *North Carolina State Univ.*
John Lach - *Univ. of Virginia*
Alper Bozkurt - *North Carolina State Univ.*
Benton Calhoun - *Univ. of Virginia*
David Wentzloff - *Univ. of Michigan*
Suman Datta, Vijay Narayanan - *Pennsylvania State Univ.*
Omer Oralkan - *North Carolina State Univ.*
Mehmet Ozturk - *Bilkent Univ.*
Jason Strohmaier - *North Carolina State Univ.*

8.2 Cognitive Cameras: Assistive Vision Systems

Vijaykrishnan Narayanan - *Pennsylvania State Univ.*
Kevin Irick - *Silicon Scapes*
Jack Sampon, Peter A. Zientra - *Pennsylvania State Univ.*

8.3 Self-powered Wearable Sensor Node: Challenges and Opportunities

Yougpan Liu, Hehe Li, Zewei Li - *Tsinghua Univ.*
Xueqing Li, Kaisheng Ma - *Pennsylvania State Univ.*
Jason Chun - *City Univ. of Hong Kong*
Sampson John - *Pennsylvania State Univ.*
Yuan Xie - *Univ. of California, San Francisco*
Huazhong Yang - *Tsinghua Univ.*

Special Session 9: CODES + ISSS - The Shift to Multicores in Real-Time and Safety-Critical Systems

Time: 14:15 - 15:30 | Room: Matterhorn 2

Chair:

Rolf Ernst - *Technische Univ. Braunschweig*

Organizer:

Selma Saidi - *Technische Univ. Braunschweig*

In real-time and safety-critical systems, the move towards multicores is becoming unavoidable in order to keep pace with the increasing required processing power and to meet the high integration trend while maintaining a reasonable power consumption. However, whereas standard multicore systems are mainly designed to increase average case performance, embedded systems have additional requirements with respect to safety, reliability and real-time behavior. Therefore, the shift to multicores raises several challenges the embedded community has to face.

These challenges involve the design of certifiable multicore platforms, the management of shared resources and the development/integration of parallel software. These issues are encountered at different steps of system development, from modeling and design to software implementation and hardware deployment. For real-time and safety critical systems, both multicore/semiconductor manufacturers and the real-time community have to bridge the gap in order to meet the challenges imposed by multicores.

9.1 Multi- and Manycores in Avionics - Challenges and Opportunities

Sascha Uhrig - *Airbus S.A.S.*

9.2 Handling Multicores In a Certified Real-Time OS

Henrik Theiling - *SYSGO*

9.3 Time-Critical Computing on the MPPA-256 Bostan Processor

Benoit Dupont de Dinechin - *Kalray Corp.*

Session 9A: EMSOFT - Formal Verification

Time: 14:15 - 15:30 | Room: Matterhorn 1

Chairs:

Timothy Bourke - *INRIA*
Indranil Saha - *Indian Institute of Technology Kanpur*

9A.1 Automatic Verification of Linear Controller Software
Miroslav Pajic - *Duke Univ.*
Junkil Park, Insup Lee, George J. Pappas, Oleg Sokolsky - *Univ. of Pennsylvania*

9A.2 Forward Invariant Cuts to Simplify Proofs for Safety
Nikos Aréchiga - *Carnegie Mellon Univ.*
James Kapinski, Jyotirmoy Deshmukh - *Toyota Technical Center*
André Platzer, Bruce Krogh - *Carnegie Mellon Univ.*

9A.3 Bounded Error Flowpipe Computation of Parameterized Linear Systems
Pavithra Prabhakar, **Ratan Lal** - *IMDEA Software Institute*

Session 9B: EMSOFT - Networked Systems

Time: 14:15 - 15:30 | Room: Zurich 1

Chairs:

Nan Guan - *Northeastern Univ.*
Tei-Wei Kuo - *Academia Sinica*

9B.1 Verifying Network Performance of Cyber-Physical Systems with Multiple Runtime Configurations
Martin Manderscheid, Gereon Weiss, Rudi Knorr - *Fraunhofer Institute for Embedded Systems and Communication Technologies*

9B.2 Using Traffic Phase Shifting to Improve AFDX Link Utilization
Renato Mancuso, Andrew Louis
Marco Caccamo - *Univ. of Illinois at Urbana-Champaign*

Panel: Embedded System Security - What Does It Change?

Time: 16:00 - 17:30 | Room: Matterhorn 1,2,3

Moderator:

Sri Parameswaran - *Univ. of New South Wales*

Organizers:

Sri Parmeswaran - *Univ. of New South Wales*
Rolf Ernst - *Technische Univ. Braunschweig*
Jörg Henkel - *KIT/Karlsruhe Institute of Technology*

Security in embedded systems has, for a long time, received little attention, both in the security and in the embedded systems communities. Embedded systems were used in closed local networks (car, aircraft) with rather fixed and well defined functionality requiring special skills to intrude and providing little benefit to the intruder, with a few prominent exceptions, such as the Stuxnet attack. This has changed in many ways: Embedded systems use open networks, they address vital functions over such networks, such as smart grid, traffic control, or ambulant medical service, and the functions and architectures become more complex and dynamic with dominant reuse and deep and global supply chains. Internet-of-Things adds volume to this development challenging the classical embedded systems approach of a thorough lab test. It appears that embedded system design must fight on all fronts, at the same time becoming a very interesting target.

However, it is not obvious how to proceed. Security needs all levels of a design: Hardware, software, networks, applications, user interface were applicable. Only looking at a subset of these levels leads to ineffective solutions.

Security is expensive, it constrains the design process, just as safety requirements have done this before, and it is not clear how much the customers are willing to pay in the form of money and inconvenience for improved security. What is the right approach under these circumstances? Given the limited amount of human and monetary resources: Are there any primary research targets, and, if so, which ones? Should we emphasize reactive or proactive approaches? How do we bring the bits and pieces together? And specifically to industry: Are there market risks with introducing embedded system security?

Panelists:

Georg Sigl - *Technische Univ. München*
Mark Steigemann - *NXP Semiconductors*
Nathalie Feyt - *Thales*
Oleg Sokolsky - *University of Pennsylvania*

Thursday, October 8 Workshop Schedule

Fifth Workshop on Design, Modeling and Evaluation of Cyber Physical Systems (CyPhy'15)
8:30 - 17:00 | Room: Luzern

Eleventh Workshop on Embedded and Cyber-Physical Systems Education (WESE'15)
8:30 - 17:00 | Room: Lausanne

Tenth Workshop on Embedded Systems Security (WESS 2015)
8:30 - 17:00 | Room: Winterthur

Fifth Embedded Operating Systems Workshop (EWiLi'15)
8:30 - 17:00 | Room: St. Gallen

First International Workshop on Resiliency in Embedded Electronic Systems (REES 2015)
8:30 - 17:00 | Room: Monte Rosa

10:00 - 10:30 Coffee (Atrium Foyer)

12:00 - 13:30 Lunch (Atrium Foyer + Zurich 2)

15:00 - 15:30 Coffee (Atrium Foyer)

Workshop: 10th Workshop on Embedded Systems Security (WESS 2015)

Time: 8:30 - 17:00 | Room: Winterthur

Embedded computing systems are continuously adopted in a wide range of application areas and importantly, they are responsible for a large number of safety-critical systems as well as for the management of critical information. The advent of the Internet-of-Things introduces a large number of security issues: the Internet can be used to attack embedded systems and embedded systems can be used to attack the Internet. Furthermore, embedded systems are vulnerable to many attacks not relevant to servers because they are physically accessible. Inadvertent threats due to bugs, improper system use, etc. can also have effects that are indistinguishable from malicious attacks.

This workshop will address the range of problems related to embedded system security. Of particular interest are security topics that are unique to embedded systems. The workshop will provide proceedings to the participants and will encourage discussion and debate about embedded systems security.

Steering Committee

Catherine Gebotys - *U. Waterloo*
Dimitrios Serpanos - *QCRI*
Marilyn Wolf - *Georgia Tech*

Workshop Chairs

Stavros Koubias - *Univ. of Patras*
Thilo Sauter - *Donau University Krems*

Advanced Program:

08:30 - 10:00: Plenary talk
10:00 -10:30: Coffee Break
10:30 - 12:00: Session I: Hardware vulnerabilities and defenses
12:00 - 13:30: Lunch
13:30 - 15:00: Session II: Embedded software and protocol security
15:00 - 15:30: Coffee Break
15:30 - 17:00: Special Session: Security of Industrial Control Systems

Workshop: 1st International Workshop on Resiliency in Embedded Electronic Systems (REES 2015)

Time: 8:30 - 17:00 | Room: Luzern

With the sheer complexity of hardware and software systems, resiliency became a major challenge in embedded systems design, manufacturing, and operation. For industrial applications several standards such as ISO26262, IEC61508 or DO-254 prescribe a well-defined level of reliability, robustness, and fault-tolerance.

This joint academic/industry workshop addresses all resiliency aspects in hardware and software systems design and operation from different embedded system areas such as automotive, avionics, and industry automation. This includes, but is not limited to, design bugs and cross-layer and cross-domain design techniques from software (applications, operating systems, middleware) to hardware (system, architecture, circuits, device level). Of special interest are design-for-resiliency technologies, resilient-specific design flows, like integrated functional/stochastic approaches, and development frameworks for robust designs, such as virtual prototyping approaches, which support early evaluations and estimations to obtain high reliability with less cost.

Organizers:

Daniel Müller-Gritschneder - *Technical University of Munich, Germany*
Wolfgang Müller - *Heinz Nixdorf Institute/University of Paderborn, Germany*
Subhasish Mitra - *Stanford University CA, USA*

Advanced Program

08:30: Welcome and Introduction

08:45: Industrial Needs - Virtual Stress Tests for Advanced Motion Control Systems
A. von Schwerin- *Siemens (DE)*

Session 1: Resilient System Design *(short presentations- 3min)*

09:15: 1-1: CLEAR: Cross-Layer Exploration for Architecting Resilience
E.Cheng[1], L.G.Szafaryn[2], S.Mirkhani[1], H.Cho[1], C.-Y.Cher[3], K.Skadron[2], M.Stan[2], K. Lilja[4], J.A. Abraham[5], P.Bose[3], S.Mitra[1] *[1]Stanford U (US), [2]U Virginia (US), [3]IBM (US), [4]Robust Chip, Inc.(US), [5]UT Austin (US)*

1-2 Cross-Layer Resilience Mechanisms to Protect the Communication Path in Embedded Systems
T.Stumpf[1], H.Härtig[1], E.A.Rambo[2], R.Ernst[2] - [1]TU Dresden (DE), [2]TU Braunschweig (DE)

1-3 Reliability-Aware Task Mapping on Many-Cores with Performance Heterogeneity
K.-H.Chen[1], J.-J.Chen[1], F.Kriebel[2], S.Rehman[2], M.Shafique[2], J.Henkel[2] *- [1]TU Dortmund (DE), [2]KIT (DE)*

1-4 Providing Flexible and Reliable on-Chip Network Communication with Real-Time Constraints
E.A. Rambo, R.Ernst - *TU Braunschweig (DE)*

1-5 Reliability and Thermal Challenges in 3D Integrated Embedded Systems
Ch.Weis, M.Jung, N.Wehn - *U Kaiserslautern (DE)*

1-6 Improving Code Generation for Software-based Error Detection
N.A. Rink, J.Castrillon - *TU Dresden (DE)*

Workshop: 1st International Workshop on Resiliency in Embedded Electronic Systems (REES 2015)

Time: 8:30 - 17:00 | Room: Monte Rosa

1-7 Resilient System Design through Symbolic Simulation and Online Diagnostics Methods
T.Purusothaman, C.Radojicic, Ch.Grimm - *TU Kaiserslautern (DE)*

1-8 Checkpointing Virtualized Mixed-Critical Embedded Systems
M.Psarakis, A.Sari - *U Piraeus (GR)*

1-9 Methods of Timing Reliability Improvement for Combinational Blocks in Microelectronics Systems
S.Gavrilov, G.Ivanova – *Institute for Design Problems in Microelectronics of RAS (RU)*

09:45: Coffee Break and Poster Discussions (Poster 1.1-1.9)

Session 2: Industrial Methods

10:45: 2-1 Virtual Prototyping of Signal Processing ASICs with Error Injection Capabilities
A.Mauderer, J.-H.Oetjens - *Bosch (DE)*

11:15: 2-2 Bridging the Gap Between Probabilistic Safety Analysis and Fault Injection in Virtual Prototypes
M.Chaari, B.-A.Tabacaru, W.Ecker, C.Novello, Th.Kruse - *Infineon (DE)*

11:45: 2-3 Fully Integrated PVT Detection and Impedance Calibration System Design for Automotive Applications
V.Melikyan, A.Balabanyan, A.Durgaryan, V.Galstyan, A.Hayrapetyan - *Synopsys Armenia CJSC (AM)*

12:15: Lunch

Session 3: Automotive System Design with ISO26262

13:30: 3-1 Using YOGITECH fRTools to Efficiently Satisfy ISO26262 Requirements for Safety Analysis and Verification
R.Mariani - *YOGITECH SpA (I) – ISO 26262-11 part leader*

14:00: 3-2 ISO26262 System Compliant Architectures
L.van Dijk – *NXP (NL)*

Session 4: Resiliency Analysis Methods *(short presentations- 3min)*

14:30: 4-1 Using Virtual Platform for Reliability and Robustness Analysis of HW/SW Embedded Systems
Reda Nouacer[1], Manel Djemal[2], Smail Niar[2] - *[1]CEA/LIST (FR), [2] LAMIH U (FR)*

4-2 Testing the Resilience of Fail-Operational Systems Early On with Non-Intrusive Data Seeding
J.Fröhlich[1], J.Frtunikj[2], A.Knoll[3] - *[1]Siemens AG (DE), [2]fortiss (DE), [3]TU München (DE)*

4-3 A HW-dependent Software Model for Cross-Layer Fault Analysis in Embedded Systems
Ch.Bartsch, C.Villarraga, D.Stoffel, W.Kunz – *U Kaiserslautern (DE)*

4-4 Component Fault Localization using Built-In Current Sensors for Error Resilient Computation
S.Potluri[1], A. Satya Trinadh[2], S.Saraf[3], K.Veezhinathan[3] - *[1]TU of Denmark (DK), [2]IIT Hyderabad (India), [3]IIIT Madras (IN)*

4-5 Efficient Fault Emulation through Splitting Combinational and Sequential Fault Propagation
R.Nyberg[1], J.Heyszl[1], G.Sigl[2], *[1]Fraunhofer AISEC (DE), [2]TU München (DE)*

4-6 Graph Guided Error Effect Simulation
J.Laufenberg[1], S.Reiter[2], A.Viehl[2], O.Bringmann[1], W.Rosenstiel[1] - *[1]U Tübingen (DE), [2]FZI (DE)*

4-7 Towards Generating Test Suites with High Functional Coverage for Error Effect Simulation
A.Windhorst, H.M. Le, D.Große, R.Drechsler - *U Bremen (DE)*

Workshop: 1st International Workshop on Resiliency in Embedded Electronic Systems (REES 2015)

Time: 8:30 - 17:00 | Room: Monte Rosa

4-8 Accurate Cache Vulnerability Modeling in Presence of Protection Techniques
Y.Ko[1], R.Jeyapaul[2], Y.Kim[1], K.Lee[1],A.Shrivastava[3] - *[1]Yonsei U (KR), [2]ARM Research (US), [3]Arizona State U (US)*

4-9 On the Correlation of HW Errors and SW faults
W.Mueller[1], L.Wu[1], Ch.Scheytt[1], M.Becker[2], S. Schönberg[2] - *[1]Heinz Nixdorf Institute (DE), [2]C-LAB (DE)*

15:00 Coffee Break and Poster Discussions (Poster 4.1-4.9)

Session 5: Test, Analysis and Error Injection *(short presentations- 3min)*

15:45: 5-1 Aging Aware Timing Analysis Incorporated into a Commercial STA Tool
S.Karapetyan, U.Schlichtmann - *TU München (DE)*

5-2 An FPGA-based Testing Platform for the Validation of Automotive Powertrain ECU
L.Sterpone, D.Sabena, L.Venditti - *Politecnico di Torino (I)*

5-3 Incremental System Design with Cross-Layer Dependency Analysis
M.Moestl, R.Ernst - *TU Braunschweig (DE)*

5-4 Formal Failure Analysis of a Backup Protection Communication Network in a Smart Substation
W.Ahmed, O.Hasan[1], S.Tahar[2] – *[1]NUST (PK), [2]Concordia U (CN)*

5-5 ErrorPro: Software Tool for Stochastic Error Propagation Analysis
A.Morozov, R.Tuk, K.Janschek - *TU Dresden (DE)*

5-6 Fault Injection in Multi-Domain Physical System Models at Different Levels of Abstraction
R.Koppak[1], O.Bringmann[1], A. v.Schwerin[2] - *[1]U Tübingen (DE), [2]Siemens (DE)*

5-7 Comparison of Different Fault-Injection Methods into TLM Models
B.-A.Tabacaru, M.Chaari, W.Ecker, Th.Kruse, C.Novello - *Infineon (DE)*

16:05 Poster Discussions (Poster 5.1-5.7)

Closing

16:50: Workshop Wrap-up

17:00: End

Workshop: 5th Embedded Operating Systems Workshop (EWiLi'15)

Time: 8:30 - 17:00 | Room: St. Gallen

EWiLi'15, the 5th Embedded Operating System Workshop, aims at presenting state-of-the-art research, experimentations, significant and original realizations that focus on the design and implementation of embedded operating systems in both academic and industrial worlds with a special interest in Hardware / Software interactions including FPGAs.

EWiLi's two first editions were dedicated to the Embedded Linux (EWiLi stands for Embed With Linux) operating system which has progressively constituted a strong alternative to proprietary and/or commercial solutions in embedded systems, whether it is deeply embedded or not, and this for many application domains, such as multimedia, telecoms, transport, etc.

The EWiLi workshop is embedded operating system centric and includes but is not limited to the following topics:
- Embedded operating systems and education
- Methods, software and tool chains
- Model-driven engineering and embedded operating systems
- Data management and memory hierarchy optimization
- Real-time, concurrency, scheduling and temporal performance
- File systems, storage, and I/Os in embedded operating systems
- Embedded operating systems and reconfigurable architectures
- Embedded operating systems and MPSOC
- Embedded operating systems and multi-core
- Embedded operating systems and sensor networks
- Energy and power optimization in embedded operating systems
- Debugging and profiling for embedded operating systems
- Case studies and application projects
- Performance evaluation and optimization

2015's edition is held in conjunction with the Embedded Systems Week (ESWEEK) in Amsterdam, The Netherlands. The previous editions were organized in Lisbon/Portugal (2014), Toulouse/France (2013), Lorient/France (2012), and Saint Malo/France (2011).

Organizing Committee
Jalil BOUKHOBZA, Lab-STICC/University of Western Brittany
Jean Philippe DIGUET, DR CNRS, Lab-STICC/University of South Brittany
Pierre FICHEUX, CTO, Open Wide/OWI
Frank SINGHOFF, Lab-STICC/University of Western Brittany

Publicity Co-Chairs
Giuseppe LIPARI, Univ. Lilles
Duo Liu, Chongqing Univ.

Workshop: 5th Embedded Operating Systems Workshop (EWiLi'15)

Time: 8:30 - 17:00 | Room: St. Gallen

EWiLi'15 Program

08:15: Welcome

08:30 - 09:30: Keynote speaker: Pr. Tei-Wei Kuo

Session 1: Scheduling analysis

09:30 - 10:00: Performance Evaluation of RUNT Algorithm.
Hiroyuki Chishiro, Masayoshi Takasu, Rikuhei Ueda and Nobuyuki Yamasaki.

10:00 - 10:30: Coffee Break

Session 1: scheduling analysis (cont)

10:30 - 11:00: Fuzzy Logic Based Adaptive Hierarchical Scheduling for Periodic Real-Time Tasks.
Tom Springer, Steffen Peter and Tony Givargis.

11:00 - 11:30: Abstract Timers and their Implementation onto the ARM Cortex-M family of MCUs.
Per Lindgren, Marcus Lindner, Andreas Lindner, Emil Fresk, David Pereira and Luis Miguel Pinho.

11:30 - 12:00: Cache-Aware Real-Time Scheduling Simulator: Implementation and Return of Experience.
Hai Nam Tran, Frank Singhoff, Stéphane Rubini and Jalil Boukhobza.

12:30 - 13:30: Lunch

13:30 - 14:30: Keynote Speaker: Julien Marechal - *R&D engineer, Thales Group, France*
With a keynote on "Thales Communications and Security, radio communications and embedded world"

Session 2: Operating system : I/O and memory

14:30 - 15:00: Exploring Storage Bottlenecks in Linux-based Embedded Systems.
Russell Joyce and Neil Audsley.

15:00 - 15:30: Coffee Break

Session 2: Operating system : I/O and memory (cont)

15:30 - 16:00: Supporting Virtualization Standard for Network Devices in RTEMS Real-Time Operating System.
Jin-Hyun Kim, Sang-Hun Lee and Hyun-Wook Jin.

16:00 - 16:30: GCMA: Guaranteed Contiguous Memory Allocator.
Seongjae Park, Minchan Kim and Heon Y. Yeom.

Session 3: Monitoring and Adaptability

16:30 - 17:00: Autonomic Thread Scaling Library for QoS Management.
Gianluca Durelli and Marco Domenico Santambrogio.

17:00 - 17:30: Towards Integration of Adaptability and Non-Intrusive Runtime Verification in Avionic Systems.
José Rufino.

Workshop: Fifth Workshop on Design, Modeling and Evaluation of Cyber Physical Systems (CyPhy'15)

Time: 8:30 - 17:00 | Room: Luzern

Cyber physical systems (CPS) combine computing and networking power with physical components. They enable innovation in a wide range of domains including robotics; smart homes, vehicles, and buildings; medical implants; and future-generation sensor networks. CyPhy'15 brings together researchers and practitioners working on modeling, simulation, and evaluation of CPS, based on a broad interpretation of these areas, to collect and exchange expertise from a diverse set of disciplines. The workshop places particular focus on techniques and components to enable and support virtual prototyping and testing.

General Chair:

Walid Taha - *Halmstad and Rice Universities*

Program Chairs:

Christian Berger - *Chalmers and University of Gothenburg*
Mohammad Reza Mousavi - *Halmstad University*

Advanced Program

09:00-10:00: Keynote - Maurice Heemels - Resource-aware control and dynamic scheduling in CPS

10:00-10:30: Coffee / tea break

10:30-11:00: Research paper - Holger Hermanns, Jan Krcal and Gilles Nies.
Recharging Probably Keeps Batteries Alive.

11:00-11:30: Research paper - Usman Sanwal and Osman Hasan.
Formally Analyzing Continuous Aspects of Cyber-Physical Systems Modeled by Homogeneous Linear Differential Equations.

11:30-12:00: Invited paper - Sebastian Siegl and Martin Russer.
Constructive Modelling of Parallelized Environmental Models for Structured Testing of Automated Driving Systems.

12:00-13:30: Lunch

13:30-14:00: Research paper - Benjamin Beichler, Thorsten Schulz, Christian Haubelt and Frank Golatowski.
A Parametric Dataflow Model for the Speed and Distance Monitoring in Novel Train Control Systems.

14:00-14:30: Research paper - Keyur Parmar and Devesh Jinwala.
Hybrid Secure Data Aggregation in Wireless Sensor Networks.

14:30-15:00: Invited paper - Stefan Schupp, Erika Abraham, Xin Chen, Ibtissem Ben Makhlouf, Goran Frehse, Sriram Sankaranarayanan and Stefan Kowalewski.
Current Challenges in the Verification of Hybrid Systems.

15:00-15:30: Coffee / tea break

15:30-16:00: Research paper - Manuela Bujorianu and Nir Piterman.
A Modelling Framework for Cyber-Physical System Resilience.

16:00-16:30: Research paper - Shin Nakajima and Si-Mohamed Lamraoui.
Fault Localization of Energy Consumption Behavior using Maximum Satisfiability

16:30-17:00: Invited paper - Michel Reniers, Sebastian Engell, Haydn Thompson, Radoslav Paulen and Christian Sonntag.
Core Research and Innovation Areas in Cyber-Physical Systems of Systems: Initial Findings of the CPSoS Project.

Workshop: Eleventh Workshop on Embedded and Cyber-Physical Systems Education (WESE'15)

Time: 8:30 - 17:00 | Room: Lausanne

Workshop Chairs:

Martin Törngren - *KTH, chair*
Martin Edin Grimheden - *KTH, co-chair*
Falk Salewski - *Muenster University of Applied Sciences, Co -chair, dissemination*

The WESE workshop series aims to bring researchers, educators, and industrial representatives together to assess needs and share design, research, and experiences in embedded and cyber-physical systems education. Embedded and cyber-physical systems design requires multidisciplinary skills from areas such as control and signal processing theory, electronics, computer engineering and science, networking, physical systems modeling, etc., as well as application domain knowledge. Demand for embedded and cyber-physical system engineers has motivated a growing interest in the question of educating specialists in this domain. As system designs grow more complex and the time to market diminishes, quality education becomes more and more important. The technological evolution manifested by CPS thus requires a corresponding evolution of engineering education, addressing questions such as "What skills and capabilities are required by the engineers of tomorrow", and "How should the corresponding educational programs be formed", in order to provide experts ready to engineer the Cyber-Physical Systems that will greatly impact our future society?

Special attention this year will be given to industrial and societal needs. The format of the workshop apart from keynotes, include regular and work-in progress paper presentations, and ample space for discussions to promote active exchange of ideas. WESE 2015 is the 11th workshop in this series.

09.00: Welcome - Martin Törngren - *KTH Royal Institute of Technology, Sweden*

09.10: Keynote 1 - A First Course on Cyber-Physical Systems - The Flipped Classroom Experience
Walid Taha - *Halmstad University, Sweden*

10.00: Break

10.10: Paper Session 1 - A Multi-Robot Search Using LEGO Mindstorms - An Embedded Software Design Project
Paula Herber and Verena Klös - *University of Potsdam, Germany*

Preparing Students for Embedded Software Development: An RTOS-based Approach
James Archibald and Doran Wilde - *Brigham Young University, USA*

11.00: Paper Session 2 - Teaching Industrial Automation: An Approach for a Practical Lab Course
Falk Salewski and Rainer Schmidt - *Muenster University of Applied Sciences, Germany*

Teaching Mixed-Criticality: Multi-Rotor Flight Control and Payload Processing on a Single Chip
Henning Schlender et al

11.50: Lunch

13.00: Keynote 2 - Challenges of starting a new Embedded Systems Speciality in an established EE Dept.
Michael Winokur - *IAI, Israel*

Workshop: Eleventh Workshop on Embedded and Cyber-Physical Systems Education (WESE'15)

Time: 8:30 - 17:00 | Room: Lausanne

13.50: Paper Session 3 - Teaching the Internet of Things Concepts
Farha Ali - *Lander University, USA*

xCPS: A tool to eXplore Cyber Physical Systems
Shreya Adyanthaya et al

Education and training challenges in the era of Cyber-Physical Systems: beyond traditional engineering
Martin Törngren et al

15.00: Break

15.15: Poster Cyber-Physical System and Contract-Based Design - A Three Dimensional View
Hadi Zaatiti and Daniela Cancila - *CEA, France*

A Development of Educational Robot Software for Master's Course Students
Harumi Watanabe et al

Experiences with a Project to Design Autonomous Slotcars in a Mechatronics Master's Program
Peter Gober - *Beuth Hochschule für Technik Berlin, Germany*

PBL in Embedded and Real-Time Systems Design Course: A Case Study Firefighting Robots
Mustafa Engin, *Ege University, Turkey*

Systems Engineering of Cyber-Physical Systems Education Program
Jon Wade et al

17.00: End

Thursday & Friday Symposia Schedules

Thursday

	Matterhorn 2	Matterhorn 3	Matterhorn 1
8:30 - 10:00	**Symposium:** 13th IEEE Symposium on Embedded Systems for Real-Time Multimedia **(ESTIMedia 2015)**	**Symposium:** 26th IEEE International Symposium on Rapid System Prototyping **(RSP)**	
10:00 - 10:30	**Coffee (Atrium Foyer)**		
10:30 - 12:00	**Symposium:** 13th IEEE Symposium on Embedded Systems for Real-Time Multimedia **(ESTIMedia 2015)**	**Symposium:** 26th IEEE International Symposium on Rapid System Prototyping **(RSP)**	**Symposium:** Internet-of-Things Symposium **(IoT)**
12:00 - 13:30	**Lunch (Atrium Foyer + Zurich 2)**		
13:30 - 15:00	**Symposium:** 13th IEEE Symposium on Embedded Systems for Real-Time Multimedia **(ESTIMedia 2015)**	**Symposium:** 26th IEEE International Symposium on Rapid System Prototyping **(RSP)**	**Symposium:** Internet-of-Things Symposium **(IoT)**
15:00 - 15:30	**Coffee (Atrium Foyer)**		
15:30 - 17:00	**Symposium:** 13th IEEE Symposium on Embedded Systems for Real-Time Multimedia **(ESTIMedia 2015)**	**Symposium:** 26th IEEE International Symposium on Rapid System Prototyping **(RSP)**	**Symposium:** Internet-of-Things Symposium **(IoT)**

Friday

	Matterhorn 3	Lausanne
8:30 - 10:00	**Symposium:** 13th IEEE Symposium on Embedded Systems for Real-Time Multimedia **(ESTIMedia 2015)**	**Symposium:** 26th IEEE International Symposium on Rapid System Prototyping **(RSP)**
10:00 - 10:30	**Coffee (Atrium Foyer)**	
10:30 - 12:15	**Symposium:** 13th IEEE Symposium on Embedded Systems for Real-Time Multimedia **(ESTIMedia 2015)**	**Symposium:** 26th IEEE International Symposium on Rapid System Prototyping **(RSP)**

Symposium: Internet-of-Things Symposium (IoT)

Time: 10:30 - 17:00 | Room: Matterhorn 1

Chairs:

Marilyn Wolf - *Georgie Institute of Technology*
Chun Jason Xue - *City University of Hong Kong*

10:00 - 10:30: Coffee Break

Session 1: Contributed Posters

10:30 - 12:00: Farzad Samie, KIT, "New Problems and Challenges in Bandwidth Allocation for IoT"
Saad Mubeen, "Applying Mitigation Mechanisms for Cloud-based Controllers in Industrial IoT Applications"
David McCann, "Characterising and Comparing the Energy Consumption of Side Channel Attack Countermeasures and Lightweight Cryptography on Embedded Devices"
Santanu Sarma, UCI, "Essence: A Machine Learning Approach to Sensemaking for Internet-of-Things"

12:00 - 13:30: Lunch

Session 2: Invited Talks

13:30 - 14:45: Chi-Sheng Daniel Shih, National Taiwan University, "Proactive and Intelligent Middleware for User-Centric IoT Systems"
Qi Zhu, UC Riverside, "Model-based Design and Synthesis of IoT Applications"
Yongpan Liu, Tsinghua University, "Ambient Energy Harvesting Nonvolatile Processors for Internet of Things"

15:00 - 15:30: Coffee Break

15:30 - 17:00: Joint Session with WESS

Symposium: 13th IEEE Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia 2015)

THURSDAY, OCTOBER 8

Time: 8:40 - 17:00 | Room: Matterhorn 2

Multimedia plays an important role in our daily activities and has become one of the most relevant technological innovations. The evermore increasing computational and communication requirements demanded by current and next generation multimedia devices together with energy constraints which characterize portable devices require innovative design methodologies and tools. The IEEE ESTIMedia aims to bring together people from different multimedia-related research communities who have worked separately but did not interact sufficiently to address the challenges facing the design of hardware and software layers of multimedia systems.

The 13th edition of ESTIMedia is continuing to be run in the Embedded System Week and will provide a forum for researchers, from academia and industry, to present and discuss innovative ideas and solutions related to embedded systems for real-time multimedia.

8:40 - 9:00: Opening

9:00 - 10:00: Keynote - The Quest for Parallelism vs Heisenbugs - Multicore Programming from the Trenches
Dr. Martijn Rutten - *Co-founder and CEO of Vector Fabrics BV, The Netherlands*

General Chair:
Todor Stefanov - *Leiden University, The Netherlands*

Technical Program Chairs
Hyunok Oh - *Hanyang University, Korea*
Muhammad Shafique - KIT/*Karlsruhe Institute of Technology, Germany*

Abstract

Multicore is booming. Smart phones aggressively market their quad-core and octa-cores; the race towards the self-driving car forces automotive companies to go dual- and quad-core; network routers go all out on their manycores. But what about the software?

Did you ever face a veritable Heisenbug? One that if you look at it in a debugger, the bug seems to disappear? If you wrote multicore code, you'll recognize the nasty data race or deadlock. And what about creating threads to get parallel performance? Disappointed by the result? To get multicore performance right, you know you need a true ninja to deal with issues like false sharing and blocking data dependencies. In this talk, Martijn will show the true pain of going multicore. The demons that mobile and automotive vendors face, yet never speak about in public. Given the intense pain of working with millions of lines of C++, these vendors hail programming tools as the silver bullet. Only to discard them faster than lightning as snake oil.

The road to getting programming tools to these fast-moving, yet conservative companies is larded with roadblocks and unexpected turns. Building on many years of trench digging himself, Martijn will quickly convince you that a great technology plays just a tiny part.

Speaker's Bio:

Martijn Rutten is a co-founder and CEO of Vector Fabrics, relentlessly trying to improve the state of programming with multicore programming tools. As a true innovator, Vector Fabrics has pioneered a wide array of parallel programming solutions before their time: from CPU-FPGA programming in the cloud to today's Pareon toolsuite for multicore programming. Martijn has a PhD in computer science from University of Amsterdam, developed multicore SoCs at Philips Research and NXP, and filed a bunch of patents. While secretly hacking on compiler intricacies in his evenings, Martijn is now mostly found outside the office. At the customers. Hunting Heisenbugs.

Symposium: 13th IEEE Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia 2015)

10:00 - 10:30: Coffee Break

Special Session: Dynamics and Predictability in Stream Processing -- A Contradiction?
Session Chair: Frank Hannig - *Friedrich-Alexander University Erlangen-Nürnberg (FAU), Germany*

10:30 - 12:00: Predictability of Image Processing Algorithms on Heterogeneous MPSoC
Johny Paul and Walter Stechele, Technische Universität München (TUM), Germany

Invasive Computing for Predictable Stream Processing:
A Simulation-based Case Study
Sascha Roloff, Stefan Wildermann, Frank Hannig, and Jürgen Teich, Friedrich-Alexander University Erlangen-Nürnberg (FAU), Germany

Floating Point Acceleration for Stream Processing Applications in Dynamically Reconfigurable Processors
Lars Bauer, Artjom Grudnitsky, Marvin Damschen, Srinivas Rao Kerekare, and Jörg Henkel, KIT/Karlsruhe Institute of Technology, Germany

Dynamic Task Mapping of Graphics Processing Applications on Many-Core Architectures through Stream Rewriting
Christian Haubelt and Lars Middendorf, University of Rostock, Germany

12:00 - 13:30: Lunch

Session I - Task Mapping and Scheduling of Video Streaming Applications
Session Chair: Hyunok Oh - *Hanyang University, Korea*

13:30 - 14:45: Energy-Efficient Mapping of Real-Time Streaming Applications on Cluster Heterogeneous MPSoCs
Di Liu, Jelena Spasic, Gang Chen and Todor Stefanov

Bio-inspired Distributed Task Remapping for Multiple Video Stream Decoding on Homogeneous NoCs
Hashan Roshantha Mendis, Leandro Soares Indrusiak and Neil Audsley

Quasi-Static Scheduling of Data Flow Graphs in the Presence of Limited Channel Capacities
Joachim Falk, Tobias Schwarzer, Michael Glaß, Jürgen Teich, Christian Zebelein and Christian Haubelt

14:45 - 15:00: Posters Session

15:00 - 15:30: Coffee Break

Session II - Web, JavaScript, and WebRTC
Session Chair: Muhammad Shafique - *KIT/Karlsruhe Institute of Technology, Germany*

15:30 - 16:45: Framework Separated Migration for Web Applications
Jin-woo Kwon, JinSeok Oh, InChang Jeong and Soo-Mook Moon

JavaScript Ahead-of-Time Compilation for Embedded Web Platform
HyukWoo Park, Wonki Jung and Soo-Mook Moon

WebRTCBench: A Benchmark for Performance Assessment of WebRTC Implementations
Sajjad Taheri, Laleh Aghababaie Beni, Rosario Cammarota, Alexander Veidenbaum, Alexandru Nicolau, Jianlin Qiu, Qiang Lu and Mohammad Haghighat

16:45 - 17:00: Posters

Symposium: 13th IEEE Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia 2015)

FRIDAY, OCTOBER 9

Time: 8:30 - 12:05 | Room: Matterhorn 3

Session III: Modeling, Energy Minimization, and Reservations for Real-Time Systems
Session Chair: KyoungWoo Lee - *Yonsei University, Korea*

8:30 - 9:45: Mode-Controlled Data-Flow Modeling of Real-Time Memory Controllers
Yonghui Li, Hrishikesh Salunkhe, João Bastos, Orlando Moreira, Benny Akesson and Kees Goossens

On-the-fly Energy Minimization for Multi-Mode Real-Time Systems on Heterogeneous Platforms
Adrian Lifa, Petru Eles and Zebo Peng

Adaptive Multi-Resource End-to-End Reservations for Component-Based Distributed Real-Time Systems
Nima Khalilzad, Mohammad Ashjaei, Moris Behnam, Luís Almeida and Thomas Nolte

9:45 - 10:00: Posters

10:00 - 10:30: Coffee Break

Session IV: Security and Recognition for Video Applications and Governor for Mobile Game
Session Chair: Todor Stefanov - *Leiden University, The Netherlands*

10:30 - 11:45: Integrated Visual Security Management for Video Encryption in Limited Battery Devices
JunHyung Moon and KyoungWoo Lee

Visual Co-occurrence Network : Using Context for Large-scale Object Recognition in Retail
Siddharth Advani, Brigid Smith, Yasuki Tanabe, Matthew Cotter, Kevin Irick, Jack Sampson and Vijaykrishnan Narayanan

Memory-aware Cooperative CPU-GPU DVFS Governor for Mobile Games
Chenying Hsieh, Nikil Dutt, Sung-Soo Lim and Jurn-Gyu Park

11:45 - 11:50: Closing and Best Paper Award ceremony

11:50 - 12:05: Poster Session

Symposium: 26th IEEE International Symposium on Rapid System Prototyping (RSP)

Time: 8:30 - 17:00 | Room: Matterhorn 3

The IEEE International Symposium on Rapid System Prototyping (RSP) emphasizes design experience sharing and collaborative approach between hardware and software research communities from industry and academy. It considers prototyping as an iterative design approach for embedded hardware and software systems. The RSP series of symposium aim at bridging the gaps in embedded system design between applications, architectures, tools, and technologies to achieve rapid system prototyping of emerging software and hardware systems.

For its 26th venue, the Rapid System Prototyping symposium seeks original contributions related to this target, encompassing a wide scope ranging from formal methods for the verification of software and hardware systems to case studies of emerging embedded systems and technologies. The symposium proposes a two-day inspiring international forum for discussing the latest related innovations and research activities. The symposium program will include keynote speeches and technical papers on timely topics.

THURSDAY, OCTOBER 8

8:30: Symposium Opening

Session 1 – Verification of Software-based Real-time Systems

8:40: Keynote: Toward a Space System Development Framework
Jean-Louis Terraillon, Maxime Perrotin, Christophe Honvault - *European Space Agency*

9:30: Invited Paper: Model-Based Design and Automated Validation of ARINC653 Architecture using the AADL
Jérôme Hugues - *ISAE SUPAERO Institut Supérieur de l'Aéronotique et de l'Espace, France*
Julien Delange - *Carnegie Mellon Engineering Institute, USA*

10:00: Coffee Break

Session 2 – Energy-efficient Embedded Systems

10:30: Evaluation of Energy Savings on a VLIW Processor through Dynamic Issue-width Adaptation
Juan Sebastian Piedrahita Giraldo, Anderson Sartor, Luigi Carro, Stephan Wong and Antonio Carlos Schneider Beck

11:00: Application-Specific Memory Protection Policies for Energy-efficient and Reliable Embedded Systems Design
Sheng Yang, Rishad Shafik, Geoff Merrett, Bashir M. Al-Hashimi, Saqib Khursheed and David Flynn

11:30: X-Ware: Mutant Computing Substrates
João Gabriel Reis, Lucas Wanner and Antônio Augusto Fröhlich

12:00: Lunch

Session 3 – Prototyping Frameworks and Experiences

13:30: Invited Paper: Mapping of AADL models on an ESL Virtual Platform for Performance Verification
M. Gaudron, Guy Bois - *Ecole Polytechnique de Montréal, Canada*
Jérôme Hugues - *ISAE-SUPAERO, France*

14:00: Invited paper: Design of Critical Embedded Systems: from Early Specifications to Prototypes
Arnaud Grasset – *Thalès Research & Tech - France*

14:30: ROSMOD: A Toolsuite for Modeling, Generating, Deploying, and Managing Distributed Real-time Component-based Software using ROS
Pranav Srinivas Kumar, William Emfinger, Amogh Kulkarni, Gabor Karsai, Dexter Watkins, Benjamin Gasser, Cameron Ridgewell and Amrutur Anilkumar

15:00: Coffee Break

Session 4 – Fast Prototyping and Parallelism Extraction

15:30: Fast GPU-in-the-loop Simulation Technique at OpenGL ES API level for Android Graphics Applications
Youngsub Ko, Youngmin Yi, Joongbaik Kim and Soonhoi Ha

16:00: Challenges for the Parallelization of Loosely Timed SystemC Programs
Denis Becker, Matthieu Moy and Jérôme Cornet

16:30: Dynamic Data Flow Analysis for NoC Based Application Synthesis
Matthieu Payet, Virginie Fresse, Frédéric Rousseau and Pascal Remy

17:00: CAASPER: Providing Accessible FPGA-acceleration over the Network
Valentin Mena Morales, Yahia Brakni, Pierre-Henri Horrein and Amer Baghdadi

Symposium: 26th IEEE International Symposium on Rapid System Prototyping (RSP)

Time: 8:30 - 12:15 | Room: Lausanne

FRIDAY, OCTOBER 9

Session 5 – Design and Challenges of IP-based and Cyber-physical Systems

8:30: Ensuring Safety and Reliability of IP-based System Design – A Container Approach
Arun Chandrasekharan, Kenneth Schmitz, Ulrich Kühne and Rolf Drechsler

9:00: Proper Handling of Interrupts in Cyber-Physical Systems
Mateus K. Ludwich and Antônio Augusto Fröhlich

9:30: Towards an Analysis-Driven Rapid Design Process for Cyber-Physical Systems
Zsolt Lattmann, James Klingler, Patrik Meijer, Jason Scott, Sandeep Neema, Ted Bapty and Gabor Karsai

9:45: A Testbed to Simulate and Analyze Resilient Cyber-Physical Systems
Pranav Srinivas Kumar, William Emfinger and Gabor Karsai

10:00: Coffee Break

Session 6 – Prototyping Flows and Hardware/Software Partitioning

10:30: GMA: A High Speed Metaheuristic Algorithmic Approach to Hardware Software Partitioning for Low-cost SoCs
Naman Govil and Shubhajit Roy Chowdhury

11:00: Generic Scrubbing-based Architecture for Custom Error Correction Algorithms
Rui Santos, Shyamsundar Venkataraman and Akash Kumar

11:30: A Multi-Objective Approach for Software/Hardware Partitioning in Reconfigurable Embedded Systems
Ihsen Alouani, Braham Lotfi Mediouni and Smail Niar

11:45: Hard Block Reduction and Synthesis Improvements in Odin II
Bo Yan and Kenneth Kent

12:00: Rapid Prototyping of Complete Systems, the Case Study of a Smart Parking
Laurent-Frédéric Ducreux, Claire Guyon-Gardeux, Maxime Louvel, François Pacull, Safietou Raby Thior and Maria Isabel Vergara-Gallego

12:15: Symposium Closing

ESWeek Committees

ESWEEK General Chairs

General Chair: Rolf Ernst
TU Braunschweig

General Vice Chair: Jörg Henkel
KIT/Karlsruhe Institute of Technology

ESWEEK Organizational Chairs

Finance Chair
Jörg Henkel
KIT/Karlsruhe Institute of Technology

Publication Chair
Haibo Zeng
Virginia Tech

Web Chair
Aviral Shrivastava
Arizona State University

Publicity Chair
Lars Bauer
KIT/Karlsruhe Institute of Technology

Tutorials Chair
Sharon Hu
University of Notre Dame

Workshop Chair
Tulika Mitra
National University of Singapore

Industry Liaison Committee Chair
Andreas Herkersdorf
TU Munchen

Awards Chair
Petru Ion Eles
Linkoping University

ESWEEK Local Arrangement Chairs

Todor Stefanov
Leiden University

Andy D. Pimentel
University of Amsterdam

ESWEEK Conference Program Chairs

CASES:

Ravishankar Iyer
Intel

Siddharth Garg
NYU Polytechnic School of Engineering

CODES+ISSS:

Gabriela Nicolescu
Polytechnique Montreal

Andreas Gerstlauer
University of Texas at Austin

EMSOFT:

Alain Girault
INRIA, Grenoble

Nan Guan
Northeastern University, China

ESWEEK Steering Committee

Past Chair: Karam Chatha
Qualcomm Research

CASES:

Sri Parameswaran
UNSW

Vinod Kathail
Xilinx

CODES+ISSS:

Nikil Dutt
University of California, Irvine

Petru Ion Eles
Linkoping University

EMSOFT:

Christoph Kirsch
University of Salzburg

Wang Yi
Uppsala University

ESWEEK Professional Society Liaisons

ACM SIGBED Liaison
Raj Rajkumar
Carnegie Mellon University

ACM SIGDA Liaison
Sri Parameswaran
UNSW

IEEE CEDA/CAS Liaison
David Atienza Alonso
EPFL

IFIP Liaison
Marilyn Wolf
Georgia Tech

Conference Management
Kathy Embler, CMP
MP Associates, Inc.

CASES Committees

Program Chairs

Ravishankar Iyer
Intel

Siddharth Garg
New York University

Steering Committee

Jörg Henkel (SC Chair)
KIT/Karlsruhe Institute of Technology

Erik Altman
IBM

Vinod Kathail
Xilinx

Scott Mahlke
University of Michigan

Sri Parameswaran
University of New South Wales

Rodric Rabbah
IBM

Anand Raghunathan
Purdue University

Krishna Palem
Rice University

Technical Program Committee

Vijaykrishnan Narayanan
Penn. State University

Oliver Bringmann
TU Tuebingen

Henri-Pierre Charles
CEA

Deming Chen
UIUC

Doris Chen
Altera

Heiko Falk
Hamburg University of Technology

Björn Franke
University of Edinburgh

Ann Gordon-Ross
University of Arizona

Rajiv Gupta
UC Riverside

Mark Hempstead
Drexel University

Jörg Henkel
KIT/Karlsruhe Institute of Technology

Vijay Janapa Reddi
UT Austin

Niraj Jha
Princeton University

Andreas Krall
TU Wien

Akash Kumar
TU Dresden

Anshul Kumar
IIT Delhi

Yun (Eric) Liang
Peking University

Brett Meyer
McGill University

Walid Najjar
UC Riverside

Laura Pozzi
University of Lugano

Anand Raghunathan
Purdue University

John (Jack) Sampson
Penn. State University

Muhammad Shafique
KIT/Karlsruhe Institute of Technology

Weidong Shi
University of Houston

Aviral Shrivastava
Arizona State University

Fei Sun
Cadence

Michael Taylor
UC San Diego

Yuan Xie
UC Santa Barbara

Jiang Xu
Hong Kong University of Science and Technology

Jingling Xue
University of New South Wales

Wei Zhang
Hong Kong University of Science and Technology

Ingrid Verbauwhede
KU Leuven

Hiren Patel
University of Waterloo

Guangyu Sun
Peking University

Hai (Helen) Li
University of Pittsburgh

Pei Zhang
Carnegie Mellon

Ramesh Illikkal
Intel

Michail Maniatakos
New York University

Jun Yang
University of Pittsburgh

Hank Corporaal
TU Eindhoven

Kanishka Lahiri
AMD

EMSOFT Committees

Program Chairs

Alain Girault
INRIA

Nan Guan
Northeastern University

Program Committee

Tarek Abdelzaher
University of Illinois at Urbana Champaign

Karl-Erik Årzén
Lunds Universitet

Sanjoy Baruah
University of North Carolina at Chapel Hill

Timothy Bourke
École Normale Supérieure, Paris

Björn Brandenburg
MPI-SWS

Samarjit Chakraborty
TU München

Wenguang Chen
Tsinghua University

Patricia Derler
University of California at Berkeley

Stephen Edwards
Columbia University

Petru Eles
Linköping Universitet

Rolf Ernst
TU Braunschweig

Marc Geilen
Eindhoven University of Technology

Reinhard von Hanxleden
Christian-Albrechts-University Kiel

Connie Heitmeyer
US Naval Research Laboratory

Hermann Härtig
TU Dresden

Shinpei Kato
Nagoya University

Tei-Wei Kuo
National Taiwan University

Edward Lee
University of California at Berkeley

Xuandong Li
Nanjing University

Giuseppe Lipari
Scuola Superiore Sant'Anna

Louis Mandel
IBM Research

Florence Maraninchi
Univ. Grenoble Alpes, Verimag

Tulika Mitra
National University of Singapore

Miroslav Pajic
University of Pennsylvania

Luigi Palopoli
University of Trento

Linh Thi Xuan Phan
University of Pennsylvania

Jan Reineke
Saarland University

Partha Roop
The University of Auckland

Abhik Roychoudhury
National University of Singapore

Sandeep Shukla
Virginia Tech

Robert de Simone
INRIA

Oleg Sokolsky
University of Pennsylvania

Aviral Shrivastava
Arizona State University

Wenyao Xu
The State University of New York at Buffalo

Jason Xue
City University of Hong Kong

Jingling Xue
University of New South Wales

Sergio Yovine
University of Buenos Aires

CODES + ISSS Committees

Program Co-chairs
Gabriela Nicolescu
École Polytechnique Montréal
Andreas Gerstlauer
University of Texas at Austin

Program Committee
Mohammad Abdullah Al Faruque
University of California, Irvine
Bashir Al-Hashimi
University of Southampton
David Atienza
EPFL
Lars Bauer
KIT/Karlsruhe Institute of Technology
Giovanni Beltrame
Polytechnique Montréal
Luca Benini
University of Bologna
Reinaldo Bergamaschi
Odysci, Inc.
Paul Bogdan
University of Southern California
Eli Bozorgzadeh
University of California, Irvine
Oliver Bringmann
University of Tuebingen,
University of Tuebingen / FZI
Naehyuck Chang
SKorea Advanced Institute of Science and Technology (KAIST)
Yiran Chen
University of Pittsburgh
Kiyoung Choi
Seoul National University
Unmesh Bordoloi
Linköpings Universitet
Erwin de Kock
NXP Semiconductors
Robert Dick
University of Michigan
Gero Dittmann
IBM Research
Rainer Doemer
University of California, Irvine
Adam Donlin
Xilinx
Nikil Dutt
University of California, Irvine
Petru Eles
Linköpings Universitet
Fabrizio Ferrandi
Politecnico di Milano
Franco Fummi
University of Verona
Catherine H. Gebotys
University of Waterloo
Andreas Gerstlauer
University of Texas, Austin
Tony Givargis
University of California, Irvine
Kees Goossens
Eindhoven University of Technology
Ann Gordon-Ross
University of Florida
Soonhoi Ha
Seoul National University
Frank Hannig
University of Erlangen
Christian Haubelt
Universität Rostock
Jörg Henkel
KIT/Karlsruhe Institute of Technology
Pao-Ann Hsiung
National Chung Cheng University
Tohru Ishihara
Kyoto University
Axel Jantsch
Vienna University of Technology
Ahmed Jerraya
CEA Tech
Niraj Jha
Princeton University
Alex K. Jones
University of Pittsburgh
Soontae Kim
KAIST
Fadi J. Kurdahi
University of California, Irvine
Luciano Lavagno
Politecnico di Torino
Sébastien Le Beux
Lyon Institute of Nanotechnology
Jenq-Kuen Lee
National Tsing Hua University
Youn-Long Steve Lin
National Tsing Hua University
Roman Lysecky
University of Arizona
Enrico Macii
Politecnico di Torino
Jan Madsen
Technical University of Denmark
Grant Martin
Cadence Design Systems
Peter Marwedel
Technical University of Dortmund
Hiroki Matsutani
Keio University
Brett Meyer
McGill University
Prabhat Mishra
University of Florida
Wolfgang Mueller
University of Paderborn & University of Paderborn/C-LAB
Gabriela Nicolescu
Polytechnique Montréal
Umit Ogras
Arizona State University
Hyunok Oh
Hanyang University
Alex Orailoglu
University of California, San Diego
Maurizio Palesi
Kore University
Preeti Ranjan Panda
Indian Institute of Technology Delhi
Partha Pande
Washington State University
Sri Parameswaran
University of New South Wales
Sudeep Pasricha
Colorado State University
Massoud Pedram
University of Southern California
Andy Pimentel
University of Amsterdam
Massimo Poncino
Politecnico di Torino
Graziano Pravadelli
University of Verona

Technical Program Committee - CODES + ISSS 2015

Program Committee, continued

Frédéric Pétrot
TIMA Laboratory, Grenoble Institute of Technology

Martin Radetzki
University of Stuttgart

Sourav Roy
Freescale Semiconductor

Marco D. Santambrogio
Politecnico di Milano

Gunar Schirner
Northeastern University

Edwin Sha
University of Texas, Dallas

Zili Shao
The Hong Kong Polytechnic University

Aviral Shrivastava
Arizona State University

Todor Stefanov
Leiden University

Greg Stitt
University of Florida

Jürgen Teich
University of Erlangen

Donald Thomas
Carnegie Mellon University

Hiroyuki Tomiyama
Ritsumeikan University

Frank Vahid
University of California, Riverside

Kazutoshi Wakabayashi
NEC Corporation

Yuan Xie
Pennsylvania State University

Jiang Xu
Hong Kong University of Science and Technology

Jason Xue
City University of Hong Kong

Haibo Zeng
Virginia Tech

Zhiru Zhang
Cornell University

Jishen Zhao
University of California, Santa Cruz

Qi Zhu
University of California, Riverside

Mark Zwolinski
University of Southampton

Additional Reviewers:

Abbas Banaiyan Mofrad
Ahmed Khurshid
Ahmed Nassar
Alberto Bocca
Alessandro Danese
Andreas Becher
Andrew Nelson
Anuj Pathania
Armaiti Ardeshiricham
Bo-Cheng Charles Lai
Bowen Zheng
Bryan Donyanavard
Bryce Holton
Jian Cai
Chao Chen
Chia-Ling Yang
Christoph Gerum
Davide Patti
Debajit Bhattacharya
Devon Merrill
Farzad Samie
Greg Stitt
Hadi Brais
Hamed Tabkhi
Hanmin Park
Hanno Eichelberger
Hassan Anwar
Hongsun An
Hossein Tajik
Hyunjik Song
Imane Hafnaoui
Jacopo Panerati
Jaehyun Kim
Jing Lu
Jinghang Zhang
Joachim Falk
Jochen Streicher
Joerg Behrend
Jongho Kim
Jungkyu Hong
Lars Middendorf
Leonardo Piga
Liangpeng Guo
Lokesh Siddhu
M. Hammam Alsafrjalani
Mahesh Balasubramanian
Majid Sabbagh
Michael Engel
Michael Witterauf
Michele Lora
Moritz Schmid
Moslem Didehban
Myungjun Lee
Namhyung Kim
Nasibeh Taimouri
Neetu Jindal
Olaf Neugebauer
Pascal Libuschewski
Peng-Sheng Chen
Rahul Jain
Ramakrishna Nittala
Reinier van Kampenhout
Riccardo Cattaneo
Roger Chen-Ying Hsieh
Sandeep Chandran
Sandro Rigo
Santiago Pagani
Sean Hamilton
Sebastian Reiter
Shang-Wei Lin
Shen Feng
Stefan Müller
Sven Goossens
Tara Ghasempouri
Tiago Muck
Tianshu Wei
Udo Krautz
Ujjwal Gupta
Yebin Lee
Yooseong Kim
Yuankun Xue
Zac Blair

2015 Event Sponsors

Embedded Systems Week 2015
ESWeek.org