CASES 2015

International Conference on Compilers, Architectures and Synthesis of Embedded Systems
Oct 4-9, Amsterdam, The Netherlands

CASES 2015: Call for Papers

CASES is a forum where researchers, developers and practitioners exchange information on emerging technologies and the latest advances in compilers and architectures for high performance embedded systems design and synthesis. CASES uniquely aims to promote synergies across otherwise vertically integrated communities in embedded systems. This year, we have expanded the topic areas to cover emerging domains such as IoT and wearables and especially encourage submissions in these new areas. Previously unpublished papers containing significant novel ideas and technical results are solicited in the following areas:

Program chairs:

Ravishankar Iyer, Intel, USA
Siddharth Garg , New York University, USA

Important Dates

Abstract Submission
March 23, 2015 (11:59 pm GMT-12)

Full Paper Submission
March 30, 2015 (11:59 pm GMT-12)
(Firm deadline)

Notification of Paper Acceptance
June 08, 2015

Camera-ready version
July 13, 2015

Conference
Oct. 04-09, 2015

Areas of Interest

Previously unpublished papers containing significant novel ideas and technical results are solicited. Conference topics include, but are not limited to, the following:

Embedded Architectures: GPU and accelerator architectures, Reconfigurable processors, FPGAs and extensible cores System-on-chip (SoC) architectures, Multi-core and many-core processors for embedded computing, On-chip communication architectures and networks-on-chip, 3D architectures, integration and synthesis and Embedded system design space exploration & methodology

Compilers and Embedded Systems Software: Compilation for reliability, power, performance, Static and dynamic execution time analysis, Specification of embedded systems, Compiler support for GPUs, FPGAs and heterogeneous systems

Memory: Memory system architecture and management, Non-volatile and other emerging memory technologies, Scratchpad, smart caches and compiler controlled memories

Power, Reliability and Security: Secure architectures and hardware security, Modeling & online management of reliability, power, performance, Validation, verification & debugging of embedded software

Emerging Application Domains: Architectures/compilers for Internet of Things (IoT) platforms, Architectures/compilers for wearables and other small form factor devices, Cyber-physical systems architectures, Architectures for emerging nanoscale devices, Programmable microfluidics, Accelerators for data analytics and learning, Neuromorphic and cognitive computing

Submission Information

Papers must represent original work, not published or submitted for publication in other forums. A blind review process will be enforced. Authors must not reveal their identity directly or indirectly. Papers must be in PDF format and should not exceed **10 pages** in ACM two-column format (9pt on 8.5"x11" letter size paper). For formatting instructions and templates, visit the ACM web site. Of note, 10 pages is an upper limit. Authors are encouraged to submit shorter papers if this better fits the nature and content of the paper. Formal proceedings will be published on CD-ROM and online (Copyright held by ACM and IEEE).