Embedded Systems Week
www.esweek.org
October 7-14, 2022
Hybrid-Shanghai

CASES 2022

Call for Papers

International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES)
October 10 – October 12, 2022, Hybrid-Shanghai |Theme: AI at the Edge

CASES is a premier forum, where researchers, developers, and practitioners exchange information on the latest advances in design, optimization, validation, and applications of embedded systems, Internet of Things (IoT), and the emergent trend of integrating Artificial Intelligence into IoT (AIoT). The conference has a long tradition of showcasing leading edge research in these broad areas, covering topics including, but not limited to, hardware-software co-design and co-validation, edge intelligence, embedded architecture, memory/storage technology, security/reliability/predictability, energy-efficiency of embedded systems, and domain-specific hardware accelerators. We solicit submission of original research articles on these topics divided into five technical tracks. Each submission needs to specify one primary and one secondary track based on the relevance of the paper's technical content to the tracks.

Regular Research Paper Submissions
Abstracts: March 31, 2022
Full Papers: April 7, 2022 (firm)

Work-in-Progress (WIP) Submissions
June 11, 2022 (firm)

Notification of Acceptance
July 5, 2022 (both types)

**All submissions are due by AOE time.*

TRACK 1: AI Systems and Applications of AI at Edge
Artificial Intelligence of Things (IoT), Edge intelligence, Architectures, accelerators, and compilers for artificial intelligence hardware; Applications of machine learning algorithms and techniques to embedded systems, IoT, and Cyber-Physical Systems (CPS); Neuromorphic and cognitive computing, analytics for embedded applications; and validation techniques for AI components.

TRACK 2: Embedded Systems and IoT/CPS Security, Safety, Reliability, and Energy-Efficiency
Secure architectures, hardware security, software security for embedded systems, IoT, and CPS; Architecture, design, and compiler techniques for energy-efficiency, reliability, and aging; Modeling, analysis, and optimization for timing and predictability; Validation, verification, testing, and debugging of embedded software.

TRACK 3: Memory and Storage
Memory system architecture; Persistent memory, Emerging memory technologies (e.g., ReRAM, MRAM, FeRAM, DNA); Caches, scratchpad memory, and compiler-controlled memory; Reconfigurable memory; Processing-in-memory; and storage systems.

TRACK 4: Accelerators, Emerging Technologies, and Applications
Synthesis, optimization, and design-space exploration of high-performance, low-power accelerators; Domain-specific accelerators; Compilers for accelerators; Biologically-inspired computing; Heterogeneous and domain-specific multi-core SoC; Approximate computing; Flexible, stretchable, and flexible hybrid electronics (FHE); Augmented/virtual reality.

TRACK 5: Architectures, Compilers, System-level Design
Embedded and mobile processor micro-architecture, Multi- and many-core processors, GPU architectures, Reconfigurable computing including FPGAs and CGRAs for embedded systems and IoT/CPS, Application-Specific processor design, 3D-stacked architectures; Networks-on-Chip (NoC) architectures; on-chip communication; I/O management in embedded systems; and compiler support for CPU, GPU, reconfigurable computing, compilation for memory, storage, and on-chip communications.

Journal-integrated Publication Model: CASES 2022 has a dual publication model with five technical tracks. Regular research papers will be published in the IEEE Transactions on CAD and Work-in-Progress papers will be published in the ESWeek Proceedings. See details at http://www.esweek.org/author-information

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