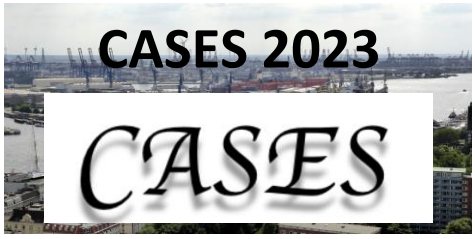

Call for Papers

International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES)
September 17 – September 22, 2023, *Hamburg, Germany*

CASES is a premier forum, where researchers, developers, and practitioners exchange information on the latest advances in design, optimization, validation, and applications of embedded systems, Internet of Things (IoT), and the emergent trend of integrating Artificial Intelligence into IoT (AIoT). The conference has a long tradition of showcasing cutting-edge research in these broad areas, covering topics including, but not limited to, hardware-software co-design and co-validation, edge AI, embedded architecture, memory/storage technology, security/reliability, energy-efficiency of embedded systems, and domain-specific hardware accelerators. We solicit submission of original research articles on these topics divided into five technical tracks. Each submission needs to specify one primary and one secondary track relevant to the paper's technical content.

Journal Track Submissions:
Abstracts: March 16, 2023
Full Papers: March 23, 2023 (firm)
Work-in-Progress Submissions:
Full Papers: May 22, 2023 (firm)
Notification of Acceptance:
June 30, 2023 (Journal track)
June 19, 2023 (WiP track)
*All submissions are due by AOE time.

TRACK 1: AI Systems and Applications of AI at Edge
Artificial Intelligence of Things (AIoT), Edge intelligence, Architectures, accelerators, and compilers for artificial intelligence hardware; Applications of machine learning techniques to embedded systems, IoT, and Cyber-Physical Systems (CPS); Neuromorphic and cognitive computing, analytics for embedded applications; and validation techniques for AI components.

TRACK 2: Embedded Systems and IoT/CPS Security, Safety, Reliability, and Energy-Efficiency
Secure architectures, hardware security, software security for embedded systems, IoT, and CPS; Architecture, design, and compiler techniques for energy-efficiency, reliability, and aging; Modeling, analysis, and optimization for timing and predictability; Validation, verification, testing, and debugging of embedded software.

TRACK 3: Memory and Storage
Memory system architecture; Persistent memory, Emerging memory technologies (e.g., ReRAM, MRAM, FeRAM, DNA); Caches, scratchpad memory, and compiler-controlled memory; Reconfigurable memory; and storage systems.

TRACK 4: Accelerators, Emerging Technologies, and Applications
Synthesis, optimization, and design-space exploration of high-performance, low-power, reliable accelerators; Domain-specific accelerators for emerging applications including AI training/inference, graph analytics, scientific computing; Compilers for accelerators; Biologically-inspired computing; Heterogeneous and domain-specific multi-core SoC; Approximate computing; Flexible hybrid electronics (FHE); Augmented/virtual reality.

TRACK 5: Architectures, Compilers, System-level Design
Embedded and mobile processor micro-architecture, Many-core processors, GPU architectures, Reconfigurable computing including FPGAs and CGRAs for embedded systems and IoT/CPS, Application-specific processor design, 3D-stacked architectures; Networks-on-Chip (NoC) architectures; I/O management in embedded systems; and compiler support for CPU, GPU, reconfigurable computing, compilation for memory, storage, and on-chip communications.

SPONSORING SOCIETIES

Journal-Integrated Publication Model: CODES+ISSS 2023 has a dual publication model with two tracks. Journal track papers will be published in ACM Transactions on Embedded Computing Systems (TECS) and Work-in-Progress track papers will be published in the ESWEEK Proceedings. See details at http://www.esweek.org/author-information

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