2023 Embedded Systems Week

17-22 September 2023 | Hamburg, Germany

2023 ESWEEK PROGRAM

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WELCOME TO ESWEEK 2023

Sharon Hu
General Chair
U. of Notre Dame, USA

Alain Girault
Vice-General Chair
INRIA, France

Heiko Falk
Local Chair
TU Hamburg, Germany

Welcome to ESWEEK 2023 in Hamburg!

Embedded Systems Week (ESWEEK) is the premier event covering all aspects of embedded systems and software. By bringing together three leading conferences (CASES, CODES+ISSS, and EMSOFT), two symposia, three hot-topic workshops, four special sessions, six tutorials, thirteen education classes, three software competitions with demos, and a special program on Diversity, Equity and Inclusion, ESWEEK presents attendees a wide range of choices unveiling state of the art embedded systems design and hardware/software architectures. Besides, ESWEEK 2023 features a special day program on the topic of semiconductor renaissance and its impact on embedded systems design.

Following the journal-integrated publication model for the three conferences (CASES, CODES+ISSS, and EMSOFT), all regular papers presented are published in the ACM Transactions on Embedded Computing Systems. In addition, authors had the possibility to publish Late Breaking papers in IEEE Embedded Systems Letters, and Work-in-Progress papers in the ESWEEK Proceedings.

The technical program on Monday, Tuesday, and Wednesday consists of 20 regular sessions and 2 special sessions from the three conferences. A strong emphasis on interaction is ensured thanks to a poster presentation for each paper, during which the participants can discuss the papers with the authors.

On Tuesday we have the semiconductor renaissance special day, focusing on the one hand on Green IoT and Green ICT for the Green Transition (the morning special session), and on the other hand on Machine Learning for Embedded System Design (afternoon special session).

Highlights of the ESWEEK program are three keynote talks by distinguished leaders in academia and industry. On Monday morning, Prof. Sarita Adve, from the University of Illinois at Urbana-Champaign, will give a talk on era of immersive computing and how it will shape the research agenda for embedded systems. Then, on Tuesday Morning, Dr. Heike Riel, IBM fellow from IBM Research Europe in Zurich, will give a talk on how to scale quantum computing. Finally, on Wednesday morning, Prof. Lothar Thiele, from ETH Zurich, will give a talk on resilient embedded systems in the era of machine learning.

Two panels will take place: An Industry Panel on Tuesday afternoon (just before the social event), dedicated to the links between the semiconductor industry and embedded computing, and an education panel on Wednesday afternoon exploring the links between computer engineering education, embedded computing, and the semiconductor renaissance.

The Test of Time Award ceremony will take place on Tuesday morning to honor the authors of articles published in previous editions of ESWEEK (respectively CASES 2008, CODES+ISSS 2007, and EMSOFT 2007), and having the highest impact. Regarding the Best Paper ceremony, it will take place on Wednesday morning, the best papers for the three conferences being selected from candidate papers presented during Monday and Tuesday regular sessions.

Thursday and Friday are the days for the symposia and workshops. We are excited to host two symposia: MEMOCODE (International Symposium on Formal Methods and Models for System Design) and NOCS (International Symposium on Networks on Chip). We are also excited to host three workshops: CODAI (Workshop on Compilers, Deployment, and Tooling for Edge AI), DOT-PIM (Workshop on Agile Design and Optimization Tools for Processing-In-Memory), and RSP (Workshop on Rapid System Prototyping).

The tutorials on Sunday precede the conferences and are an excellent opportunity to get in-depth knowledge in new trends and hot topics. There are four half-day and two full-day tutorials, covering a wide scope of topics, including high-level synthesis, model-checking, runtime monitoring and management, and hw/sw codesign. Two of these tutorials are sponsored by industry, AMD and Siemens.

On Thursday and Friday the week before (September 14th and 15th), thirteen education classes will take place, given prominent experts in embedded systems, and available virtually. These are excellent opportunities for students and young researchers to improving their knowledge in these topics.

We are grateful to our ACM (SIGBED, SIGDA, SIGMICRO) and IEEE (CEDA and CASS) sponsors as well as the following industry sponsors: AMD, NXP, Synopsys, Huawei, Bosch, and Siemens.
The organization of ESWEEK was only possible with the continuous support and help from many volunteers: The program chairs with their program committee members, the organizers of the special day, the workshops, tutorials, and symposia, all members of the organization committee, and, last but not least, the local arrangement team.

After three years of virtual conference, we are looking forward to meeting you in person at ESWEEK 2023 in Hamburg!

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Thursday, September 14	Education Classes			
	Virtual	Virtual	Virtual	Virtual
10:00-12:00	**Jian-Jia Chen** TU Dortmund **Data Flow from Cause to Effect in Distributed Systems: Data Age and Reaction**	**Preeti Ranjan Panda** IIT Delhi **3D Memory – Thermal Challenges and System Management**		
16:00-18:00	**Edward Lee** UC, Berkeley **Deterministic Concurrency and the Lingua Franca Coordination Language**	**Yiran Chen** Duke **Efficient and Robust Edge AI: Software, Hardware, and the Co-design**	**Umit Ogras** Wisconsin **A Novel Runtime Environment for Accelerator-Rich Heterogeneous Architectures**	**Aviral Shrivastava** Arizona State **Basics of Machine Learning Accelerator Design**

Friday, September 15	Education Classes			
	Virtual	Virtual	Virtual	Virtual
10:00-12:00	**Tulika Mitra** National University of Singapore **Coarse-Grained Reconfigurable Array (CGRA): Architectures and Compilers**	**Soonhoi Ha** Seoul National University **Design Methodology for Low Power Computer Vision Systems**	**Fabrizio Ferrandi** Politecnico di Milano Antonino Tumeo PNNL **High-Level Synthesis of Complex Parallel Specifications**	
16:00-18:00	**Jan Rabaey** UC, Berkeley Marian Verhelst KU Leuven **Bringing ML to the Extreme Edge**	**Sudeep Pasricha** Colorado State **Optical Computing for AI Acceleration**	**Éricles Sousa and Felipe Augusto da Silva** Cadence **The Five Must-have Features of Automotive SoC Architectures**	**Diana Goehringer** TU Dresden **Self-Adaptive Domain-Specific Computer Architectures**

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Sunday, September 17 — Tutorials and Diversity Events

	A0.18	A0.14	A1.19	A0.19	A0.13
09:00 - 10:30	**Tutorial 1: Introduction to the AMD Versal ACAP Adaptable Intelligent Engine and to its Programming Model** Mario Ruiz, Cathal McCabe, AMD	**Tutorial 2: Designing an Edge Inferencing Accelerator using High-Level Synthesis** Petri Solanti, Russell Klein, Siemens	**Tutorial 3: How to Use Model Checking to Analyze Circuits at the Transistor Level** Michael Raitza, Steffen Märcker, TU Dresden	**Tutorial 5: MARS: A framework for runtime monitoring, modeling, and management of realtime systems** Bryan Donyanavard, Biswadip Maity, Tiago Mück, UC Irvine, Arm and San Diego Univ.	
10:30 - 11:00	Coffee Break				
11:00 - 12:30	**Tutorial 1: Introduction to the AMD Versal ACAP Adaptable Intelligent Engine and to its Programming Model** Mario Ruiz, Cathal McCabe, AMD	**Tutorial 2: Designing an Edge Inferencing Accelerator using High-Level Synthesis** Petri Solanti, Russell Klein, Siemens	**Tutorial 3: How to Use Model Checking to Analyze Circuits at the Transistor Level** Michael Raitza, Steffen Märcker, TU Dresden	**Tutorial 5: MARS: A framework for runtime monitoring, modeling, and management of realtime systems** Bryan Donyanavard, Biswadip Maity, Tiago Mück, UC Irvine, Arm and San Diego Univ.	
12:30 - 13:30	Lunch Break				
13:30 - 15:00	**Tutorial 1: Introduction to the AMD Versal ACAP Adaptable Intelligent Engine and to its Programming Model** Mario Ruiz, Cathal McCabe, AMD	**Tutorial 2: Designing an Edge Inferencing Accelerator using High-Level Synthesis** Petri Solanti, Russell Klein, Siemens	**Tutorial 4: Neural Network and Autonomous Cyber-Physical Systems Formal Verification for Trustworthy AI and Safe Autonomy** Hoang-Dung Tran, Diego Manzanas Lopez, Taylor T. Johnson, Vanderbilt University	**Tutorial 6: HW/ SW Codesign for Brain-Inspired Hyperdimensional In-Memory Computing** Paul R. Genssler, Simon Thomann, Hussam Amrouch, TU Munich	**Diversity, Equity and Inclusion in Embedded Systems Research** An overview of the EUGAIN COST Action: A European Network for Gender Balance in Informatics (13h30-14h) Panel I (14h-15h): Career perspectives in academia vs. industry
15:00 - 15:30	Coffee Break				
15:30 - 17:00	**Tutorial 1: Introduction to the AMD Versal ACAP Adaptable Intelligent Engine and to its Programming Model** Mario Ruiz, Cathal McCabe, AMD	**Tutorial 2: Designing an Edge Inferencing Accelerator using High-Level Synthesis** Petri Solanti, Russell Klein, Siemens	**Tutorial 4: Neural Network and Autonomous Cyber-Physical Systems Formal Verification for Trustworthy AI and Safe Autonomy** Hoang-Dung Tran, Diego Manzanas Lopez, Taylor T. Johnson, Vanderbilt University	**Tutorial 6: HW/ SW Codesign for Brain-Inspired Hyperdimensional In-Memory Computing** Paul R. Genssler, Simon Thomann, Hussam Amrouch, TU Munich	**Diversity, Equity and Inclusion in Embedded Systems Research** Overview of the EUGAIN COST action (13h30-14h): Rukiye Altin Panel I (14h-15h): Diversity initiatives – are we on the right path? Panel II (15h30-16h30): Carreer perspectives in academia vs. industry Mentoring session (16h30-17h)
18:00 - 19:30	Reception in the ESWEEK Lunch & Coffee Area in Building A				

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Monday, September 18

8:30 - 9:00	Opening Session (Audimax 1)			
9:00 - 10:00	**KEYNOTE 1** (Audimax 1) Enabling the Era of Immersive Computing: A Rich Agenda for Embedded Systems Research Prof. Sarita Adve (UIUC)			
10:00 - 10:30	Coffee Break			
	A0.13	**H0.01+H0.02**	**H0.16**	**H0.03**
10:30 - 12:00	**CASES 1: Co-Design for ML Accelerators ***	**CODES 1: In-Memory Computing meets EdgeAI ***	**EMSOFT 1: Formal CPS design ***	**Image/AI and ESSC competitions**
10:30-10:55	Let Coarse-Grained Resources Be Shared: Mapping Entire Neural Networks on FPGAs *Best paper candidate.*	Overflow-free compute memories for edge AI acceleration *Best paper candidate.*	Towards Building Verifiable CPS using Lingua Franca.	Segmentation Track: Low-Power Computer Vision Challenge **(10:30 – 10:38)** ENOT **(10:38 – 10:46)** AidgetRock **(10:46 – 10:54)** ModelTC
10:56-11:21	MaGNAS: A Mapping-Aware Graph Neural Architectural Search Framework for Heterogeneous MPSoC Deployment	CRIMP: Compact & Reliable DNNs Inference for In-Memory Processing via Crossbar-Aligned Compression and Non-ideality Adaptation	Equation-Directed Axiomatization of Lustre Semantics to Enable Optimized Code Validation *Best paper candidate.*	Classification Track: Fair and Intelligent Embedded System Challenge **(10:54 – 11:02)** Intelligent and Robotic Systems **(11:02 – 11:10)** Sustainable Computing Laboratory **(11:10 – 11:18)** Rutgers Efficient AI
11:22-11:47	GHOST: A Graph Neural Network Accelerator using Silicon Photonics	SpinBayes: Algorithm-Hardware Co-Design for Uncertainty Estimation Using Bayesian In-Memory Approximation on Spintronic-Based Architectures	Verified Compilation of Synchronous Dataflow with State Machines *Best paper candidate.*	ESSC Competition Track 1: **(11:20 – 11:28)** gem5-NVDLA: A Simulation Framework for Compiling, Scheduling and Architecture Exploration on AI System-on-Chips **(11:28 – 11:36)** ESP: an Open-Source Platform for the Design and Programming of Heterogeneous SoCs **(11:36 – 11:44)** ARM-CO-UP: ARM Co-Operative Utilization of Processors **(11:44 – 11:52)** ZoneTrace: A Zone Monitoring Tool for F2FS on ZNS SSDs **(11:52 – 12:00)** AutoDiCE Toolkit: Fully Automated Distributed CNN Inference at the Edge
11:48-11:53	WiP: Error-Compensation-Based Energy-Efficient MAC Unit for CNNs	LB: Differentiable Slimming for Memory-Efficient Transformers	WiP: Searching Optimal Compiler Optimization Passes Sequence for Reducing Runtime Memory Profile using Ensemble Reinforcement Learning	
11:54-11:59	WiP: QRCNN: Scalable CNNs		WiP: Mixing computation and interaction on FPGA	
12:00 - 12:30	Poster Session			
12:30 - 13:30	Lunch Break			
13:30 - 15:00	**CASES 2: Edge Computing**	**CODES 2: Advanced Trends in Efficient Inference ***	**EMSOFT 2: Mobile and resource-constrained systems ***	**ESSC and SRC competitions**

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Monday, September 18 (continued)

	A0.13	H0.01+H0.02	H0.16	H0.03
13:30-13:55	Energy-efficient Personalized Federated Search with Graph for Edge Computing	Florets for Chiplets: Data Flow-aware High-Performance and Energy-efficient Network-on-Interposer for CNN Inference Tasks *Best paper candidate.*	DaCapo: An On-Device Learning Scheme for Memory-Constrained Embedded Systems	ESSC Competition Track 2: **(13:30 – 13:38)** Fault Attack Exploitability Detection in Block Cipher Softwares **(13:38 – 13:46)** HyboGen : A compiler for innovative interleaved execution and compilation scenarios **(13:46 – 13:54)** CPSim: Simulation and Security Toolbox for Cyber-Physical Systems **(13:54 – 14:02)** CHARM: Composing Heterogeneous AcceleRators for End-to-end Deep Learning Inference on Versal ACAP Architecture
13:56-14:21	ViT4Mal: Lightweight Vision Transformer for Malware Detection on Edge Devices	Keep in Balance: Runtime-reconfigurable Intermittent Deep Inference *Best paper candidate.*	iAware: Interaction Aware Task Scheduling for Reducing Resource Contention in Mobile Systems	
14:22-14:47	CIM: A Novel Clustering-based Energy-Efficient Data Imputation Method for Human Activity Recognition	STADIA: Photonic Stochastic Gradient Descent for Neural Network Accelerators	Rectifying Skewed Kernel Page Reclamation in Mobile Devices for Improving User-Perceivable Latency *Best paper candidate..*	
14:48-14:53	WiP: Towards Evaluating CNNs Against Integrity Attacks on Multi-tenant Computation	LB: DynaFuse: Dynamic Fusion for Resource Efficient Multi-modal Machine Learning Inference	LB: Efficient Partial Weight Update Techniques for Lightweight On-Device Learning on Tiny Flash-Embedded MCUs	
14:54-14:59	WiP: Automatic DNN Deployment on Heterogeneous Platforms: the GAP9 Case Study		WiP: CLERR: A High-performance Cross-layer Method for Eliminating Rendering Redundancy in Android	
15:00 - 15:30	Poster Session & Coffee Break			
15:30 - 17:00	**SS 1: Non-Volatile Memories: Challenges and Opportunities for Embedded System Architectures with Focus on Machine Learning Applications**	**CODES 3: Emerging Embedded Applications – Sustainability, Safety and Learning**	**EMSOFT 3: Networking**	**SRC: ACM Student Research Competition**
15:30-15:55	Embedded Systems with Nonvolatile Main Memories - Programming for persistence and memory access time trade-offs	A Self-Sustained CPS Design for Reliable Wildfire Monitoring	CrossTalk: Making Low-Latency Fault Tolerance Cheap by Exploiting Redundant Networks	
15:56-16:21	Architecture to compiler co-optimization for computation in resistive non-volatile memories	BASS: Safe Deep Tissue Optical Sensing for Wearable Embedded Systems	Improving worst-case TSN communication times of large sensor data samples by exploiting synchronization	
16:22-16:47	Memory-Centric Machine Learning	FedHIL: Heterogeneity Resilient Federated Learning for Robust Indoor Localization with Mobile Devices	B-AWARE: Blockage Aware RSU Scheduling for 5G Enabled Autonomous Vehicles	
16:48-16:53	Prospects of Memory-Centric Computing on Flash Memories	WiP: Efficient Gait Trajectory Prediction Method Based on Soft Constraint Weighted Template Matching	WiP: Efficient TSN network interface handling in a mixed criticality system	
16:54-16:59		WiP: NAPMAE: Generalized Data-Efficient Neural Architecture Predictor with Masked Autoencoder	WiP: Flexible bus arbitration in mixed criticality systems	
17:00 - 17:30	Poster Session			
17:30 - 19:00	Ph.D Forum (A0.18) and Recruitment Event (A0.19)			

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Tuesday, September 19

8:30 - 9:00	Test of Time Award Ceremony (Audimax 1)			
9:00 - 10:00	**KEYNOTE 2** (Audimax 1) Scaling Quantum Computing Dr. Heike Riel (IBM)			
10:00 -10:30	Coffee Break			
	A0.13	**H0.01+H0.02**	**H0.16**	**H Audimax 1**
10:30 - 12:00	**CASES 3: Embedded Systems Security***	**CODES 4: Efficient Memory Design and Management**	**EMSOFT 4: Real-Time and distributed systems**	**Special Day SS1: Green IoT and Green ICT for the Green Transition: Challenges, Opportunities, Recent Research**
10:30-10:55	Protection Window Based Security-Aware Scheduling against Schedule-Based Attacks *Best paper candidate.*	WARM-tree: Making Quadtrees Write-efficient and Space-economic on Persistent Memories	Methods to Realize Preemption in Phased Execution Models	**(10:30-10.53)** Policy implications for the energy transition: Challenges and opportunities from a system perspective
10:56-11:21	Predictable GPU Wavefront Splitting for Safety-Critical Systems	IOSR: Improving I/O Efficiency for Memory Swapping on Mobile Devices Via Scheduling and Reshaping	Consistency vs. Availability in Distributed Cyber-Physical Systems	**(10.53-11:15)** Applying Green IoT digitalization for the Green Transition: Research challenges and opportunities
11:22-11:47	PReFeR: Physically Related Function based Remote Attestation Protocol	CABARRE: Request Response Arbitration for Shared Cache Management	Probabilistic Reaction Time Analysis	**(11:15-11:37)** Digitalization in action: Use cases and lessons learned
11:48-11:53	LB: LOCoCAT: Low-Overhead Classification of CAN bus Attack Types	LB: NvMISC: Towards an FPGA-based Emulation Platform for RISC-V and Non-volatile Memories	LB: External Timed I/O Semantics Preserving Utilization Optimization for LET-based Effect Chain	**(11:37-12:00)** Green ICT for energy-efficient data centers, edge AI and IoT systems
11:54-11:59	LB: Flipping Bits Like a Pro: Precise Rowhammering on Embedded Devices	LB: CNN Workloads Characterization and Integrated CPU-GPU DVFS Governors on Embedded Systems		
12:00 - 12:30	Poster Session			

TTA Awards

Predictable Programming on a Precision Timed Architecture (CASES 2008) by *Ben Lickly, Isaac Liu, Sungjun Kim, Hiren D. Patel, Stephen A. Edwards*, and *Edward A. Lee.*

Predator: A Predictable SDRAM Memory Controller (CODES+ISSS 2007) by *Benny Akesson, Kees Goossens*, and *Markus Ringhofer.*

Scheduling Multiple Independent Hard-Real-Time Jobs on a Heterogeneous Multiprocessor (EMSOFT 2007) by *Orlando Moreira, Frederico Valente*, and *Marco Bekooij.*

All times are Central European Summer Time (CEST)

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Tuesday, September 19 (continued)

	A0.13	H0.01+H0.02	H0.16	H Audimax 1
12:30 - 13:30	Lunch Break			
13:30 - 15:00	**CASES 4: Efficient Memory Systems ***	**CODES 5: Security and Reliability**	**EMSOFT 5: Optimization and design of embedded systems**	**Special Day SS2: Machine Learning for Embedded System Design**
13:30-13:55	ZPP: A Dynamic Technique to Eliminate Cache Pollution in NoC based MPSoCs *Best paper candidate.*	Thermal Management for 3D-Stacked Systems via Unified Core-Memory Power Regulation.	Sound Mixed Fixed-Point Quantization of Neural Networks	**(13:30-14:00)** ML for System-Level Modeling and Design Speaker: Andreas Gerstlauer, UT Austin
13:56-14:21	EMS-I: An Efficient Memory System Design with Specialized Caching Mechanism for Recommendation System Inference	ANV-PUF: Machine-Learning-Resilient NVM-Based Arbiter PUF	A Constructive State-based Semantics and Interpreter for a Synchronous Data-flow Language with State machines	**(14:00-14:30)** ML for High-Level Synthesis: Opportunities and Lessons
14:22-14:47	Proactive Stripe Reconstruction to Improve Cache Use Efficiency of SSD-Based RAID Systems	HEPHAESTUS: Codesigning and Automating 3D Image Registration on Reconfigurable Architectures	Optimal Synthesis of Robust IDK Classifier Cascades	**(14:30-15:00)** Synthesis Prediction: Use Deep Learning to Expedite the Hardware Architecture and Design Process
14:48-14:53	LB: Swift-CNN: Leveraging PCM Memory's Fast Write Mode to Accelerate CNNs	LB: Effects of Runtime Reconfiguration on PUFs Implemented as FPGA-based Accelerators	LB: Optimized Local Path Planner implementation for GPU-accelerated embedded systems	
14:54-14:59	LB: No-Multiplication Deterministic Hyperdimensional Encoding for Resource-Constrained Devices	LB: Hardware-Software Co-optimization of Long-Latency Stochastic Computing	WiP: Unishyper, A Reliable Rust-based Unikernel for Embedded Scenarios	
15:00 - 15:30	Poster Session & Coffee Break			
15:30 - 17:00	**Industry Panel** (H Audimax 1) The Global Semiconductor Renaissance and Embedded Computing: An Industry Perspective Panelists: Sankar Basu (US NSF), Tobias Helbig (NXP), Heike Riel (IBM), Jin Yang (Intel), Marilyn Wolf (moderator, University of Nebraska -- Lincoln)			
17:00 - 18:00	ESSC Demo Session (H0.03)			
19:30 - 23:00	Social Event (Dinner cruise on a "Southern Style" ship)			

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Wednesday, September 20

8:30 - 9:00	Best Paper Award Ceremony		
9:00 - 10:00	**KEYNOTE 3:** The quest for resilient embedded systems in the era of machine learning Prof. Lothar Thiele (ETH)		
10:00 - 10:30	Coffee Break		
	A0.13	**H0.01+H0.02**	**H0.16**
10:30 - 12:00	**CASES 5: Approximate Computing**	**CODES 6: Data Management for Magnetic Devices**	**EMSOFT 6: Learning from black-box components**
10:30-10:55	AxOTreeS: A Tree Search Approach to Synthesizing FPGA-based Approximate Operators	LaDy: Enabling Locality-aware Deduplication Technology on Shingled Magnetic Recording Drives	Mining Hyperproperties using Temporal Logics
10:56-11:21	VADF: Versatile Approximate Data Formats for Energy-Efficient Computing	FSIMR: File-system-aware Data Management for Interlaced Magnetic Recoding	Kryptonite : Worst-Case Program Interference Estimation on Multi-Core Embedded Systems
11:22-11:47	Modular DFR: Digital Delayed Feedback Reservoir Model for Enhancing Design Flexibility	LB (11:22-11:27): Should We Even Optimize for Execution Energy? Rethinking Mapping for MAGIC Design Style	Probabilistic Black-Box Checking via Active MDP Learning
11:48-11:53	LB: Vector-Based Dedicated Processor Architecture for Efficient Tracking in VSLAM Systems	WiP: A Universal Instrumentation Platform for Non-Volatile Memories	WiP: Micro-Accelerator-in-the-Loop Framework for MCU Integrated Accelerator Peripheral Fast Prototyping
11:54-11:59	LB: An Approximate Parallel Annealing Ising Machine for Solving Traveling Salesman Problems	WiP: A Generic Non-Intrusive Parallelization Approach for SystemC TLM-2.0-based Virtual Platforms	
12:00 - 12:30	Poster Session		
12:30 - 13:30	Lunch Break		

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Wednesday, September 20 (continued)

	A0.13	H0.01+H0.02	H0.16
13:30 - 15:00	**CASES 6: Design, Management, and Security of SoCs**	**SS 2: Mitigating side-channel attacks: A multilayer bottom-up approach**	**EMSOFT 7: Design of control systems**
13:30-13:55	SpikeHard: Efficiency-Driven Neuromorphic Hardware for Heterogeneous Systems-on-Chip	(13:30-13:53) Designing SCA-resilient Circuits with Emerging Reconfigurable Nanotechnologies	Stochastic Analysis of Control Systems Subject to Communication and Computation Faults
13:56-14:21	DTRL: Decision Tree-based Multi-Objective Reinforcement Learning for Runtime Task Scheduling in Domain-Specific System-on-Chips	(13:53-14:15) Tools for Automated Generation of SCA-Protected Circuits Presenters: Amir Moradi, Ruhr University Bochum, Germany	Formal Synthesis of Neural Barrier Certificates for Continuous Systems via Counterexample Guided Learning
14:22-14:47	ObNoCs: Protecting Network-on-Chip Fabrics Against Reverse-Engineering Attacks	(14:15-14:37) Obfuscation against Side-Channel Attacks in Edge Environments Presenters: Chongzhou Fang, Ning Miao, Han Wang, Sai Manoj, Houman Homayoun, UC Davis	Neural Abstraction-Based Controller Synthesis and Deployment
14:48-14:53	LB: High Flexibility Designs of Quantized Runtime Reconfigurable Multi-precision Multipliers	(14:37-15:00) Industry Perspectives on Side-Channel Attacks and Defenses Presenters: Benjamin Hettwer, Robert Bosch Corporate Research	WiP: Integrating WebAssembly into Service Oriented Architectures for Edge Systems
14:54-14:59	LB: FPGA Implementation of Modified SNOW 3G Stream Ciphers using Fast and Resource Efficient Substitution Box		
15:00 - 15:30	Poster Session & Coffee Break		
15:30 - 17:00	**CASES 7: Co-design for ML accelerators**		**Education Panel (H0.16)**
15:30-15:55	Computationally Efficient DNN Mapping Search Heuristic using Deep Reinforcement Learning		**Computer Engineering Education, Embedded Computing, and the Semiconductor Renaissance** Panelists: Robert Dick (University of Michigan), Patrick Haspel (Synopsys), Jan Madsen (moderator, Danish Technical University), Muhammad Shafique (NYU), Marilyn Wolf (University of Nebraska -- Lincoln), Wang Yu (Tsinghua University)
15:56-16:21	DASS: Differentiable Architecture Search For Sparse neural networks		
16:22-16:47	BitSET: Bit-Serial Early Termination for Computation Reduction in Convolutional Neural Networks		
16:48-16:53			
16:54-16:59			

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Thursday, September 21 — Symposia and Workshops

	H0.01+H0.02	H0.16	H0.03	H0.07	H0.08
	MEMOCODE	**NOCS**	**Workshop DOT-PIM**	**Workshop CODAI (11:00 - 19:00)**	**Workshop RSP**
9:00 - 10:00	**Keynote 1:** Edward A. Lee (U.C. Berkeley)	**Keynote 1:** Axel Jantsch (TU Wien)	**Keynote:** Memory-Centric Computing **(9:45-10:15)** Full-stack Deployment and Design tools for RRAM-based Compute-in-memory System	**(10:35 – 11:15) Keynote:** Next-generation Compilers for Emerging Systems	**Keynote:** Digital Hardware Acceleration for Neural Networks: Implementation Considerations
10:00 -10:30	Coffee Break				
10:30-12:30	**Technical Session 1: Machine Learning**	**Technical Session 1: High-Performance and Dynamic NoC Architectures**		**Session 1: Deployment and Optimization Techniques**	
10:30 - 11:00	Safe Integration of Learning in SystemC using Timed Contracts and Model Checking	FlooNoC: A Multi-Tbps Wide NoC for Heterogeneous AXI4 Traffic	A Neuro-Vector-Symbolic Architecture for Data- and Compute-Efficient Continual Learning, Abstract Reasoning, and Combinatorial Inference		
11:00-11:30	Hybrid Genetic Reinforcement Learning for Generating Run-Time Requirement Enforcers	Dynamically Reconfigurable Network Protocol for Shape-Changeable Computer System	Opportunities and Challenges for Process-In-Memory (PIM) Technology in ICT Products	**(11:15 – 11:40)** Scaling Up Quantization-Aware Neural Architecture Search for Efficient Deep Learning on the Edge	Fast and Accurate Virtual Prototyping of an NPU with Analytical Memory Modeling
11:30-12:00	Robust Testing for Cyber-Physical Systems using Reinforcement Learning	PiN: Processing in Network-on-Chip (Tutotial Paper)	EDA Toolchain for Processing-in-Memory CNN Accelerators	**(11:40 – 12:05)** Tiny Machine Learning: Enabling Intelligence on Constrained Devices	The Impact of Heterogeneous Logic on Adders and Multipliers in VTR
12:00-12:30	Explaining Unsolvability of Planning Problems in Hybrid Systems with Model Reconciliation			**(12:05 – 12:30)** Hardware-Aware Network Compression: From Data to Silicon	Polynomial Formal Verification Exploiting Constant Cutwidth
12:30 - 13:30	Lunch Break				
13:30 - 15:00	**Technical Session 2: Verification and Synthesis**	**Technical Session 2: NoCs for AI Acceleration and Interposer Systems**		**Session 2: Compilation Frameworks and Techniques**	
13:30-14:00	Allocation and Scheduling of Dataflow Graphs on Hybrid Dataflow/von Neumann Architectures	A NoC-Based Spatial DNN Inference Accelerator with Memory-Friendly Dataflow	**(13:30-14:10)** HISIM: Heterogeneous Integration Simulator with 2.5D/3D Interconnect Modeling	**(13:30 – 13:55)** Accelerating Edge AI with Morpher: An Integrated Design, Compilation and Simulation Framework for CGRAs	**(13:30-13:50)** SerIOS: Enhancing Hardware Security in Integrated Optoelectronic Systems

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ESWEEK 2023 SCHEDULE AT-A-GLANCE

Thursday, September 21 (continued)	Symposia and Workshops				
	H0.01+H0.02	H0.16	H0.03	H0.07	H0.08
	MEMOCODE	NOCS	Workshop DOT-PIM	Workshop CODAI (11:00 - 19:00)	Workshop RSP
14:00-14:30	Harnessing Multiple BMC Engines together for Efficient Formal Verification	ELEMENT: Energy-efficient Multi-NoP Architecture for IMC-based 2.5D Accelerator for DNN Training	**(14:10-14:40)** Digital Computing-In-Memory Architecture and Design Automation	**(13:55 – 14:20)** Towards Rapid Exploration of Heterogeneous TinyML Systems using Virtual Platforms and TVM's UMA **(14:20 – 14:45)** ART: An Actor transition systems RunTime for enabling efficient partitioning of neural network graphs	**(13:50-14:10)** Extending Memory Compatibility with Yosys Front-End in VTR Flow **(14:10-14:30)** MRPHS: A Verilog RTL to C++ Model Compiler Using Intermediate Representations For Object-oriented, Model-driven Prototyping
14:30-15:00	Polynomial Formal Verification of KFDD Circuits	SoCProbe: Compositional Post-Silicon Validation of Heterogeneous NoC-Based SoCs	**(14:40-15:10)** Robust and Efficient Analog In-Memory-Computing Platforms for Neural Networks	**(14:45 – 15:10)** SYCL – A Modern C++ Programming Model for Accelerators	Integrating Quick Resource Estimators in Hardware Construction Framework for Design Space Exploration
15:00 - 15:30	Coffee Break				
15:30 - 17:00	**Technical Session 3: Specification and Verification**	**Technical Session 3: Routing and Deadlock Recovery in Interconnection Networks**		**Session 3: Applications**	
15:30-16:00	QTWTL: Quality Aware Time Window Temporal Logic for Performance Monitoring	A Reinforcement Learning Framework with Region-Awareness and Shared Path Experience for Efficient Routing in Networks-on-Chip	**(15:25-15:55)** Fast and Reconfigurable Sort-In-Memory System Enabled by Memristors **(15:55-16:20)** Benchmarking Framework for Non-volatile Capacitive Compute-in-Memory	**(15:40 – 16:05)** Temporal Patience: Efficient Adaptive Deep Learning for Embedded Radar Data Processing	**(15:30-15:50)** RaDaML: A Modeling Language for DO-178C High-Level Requirements in Airspace Systems **(15:50-16:10)** Security assessment of a commercial router using physical access: a case study
16:00-16:30	Model Checking Time Window Temporal Logic for Hyperproperties	SPOCK: Reverse Packet Traversal for Deadlock Recovery	**(16:20-16:45)** Towards Efficient Processing in Memory AI Systems with Cross-layer Optimization	**(16:05 – 16:30)** Pros and Cons of Executable Neural Networks for Deeply Embedded Systems **(16:30 – 16:55)** Software and Hardware for Sparse ML	**(16:10-16:30)** Fast Compiler Optimization Flag Selection **(16:30-17:00)** HDLGen and ChatGPT Case Study: RISC-V Processor VHDL and Verilog Model, Testbench and EDA Project Capture
18:15 - 23:15	Reception and Buffet Dinner (Restaurant Leuchtturm)				

All times are Central European Summer Time (CEST)

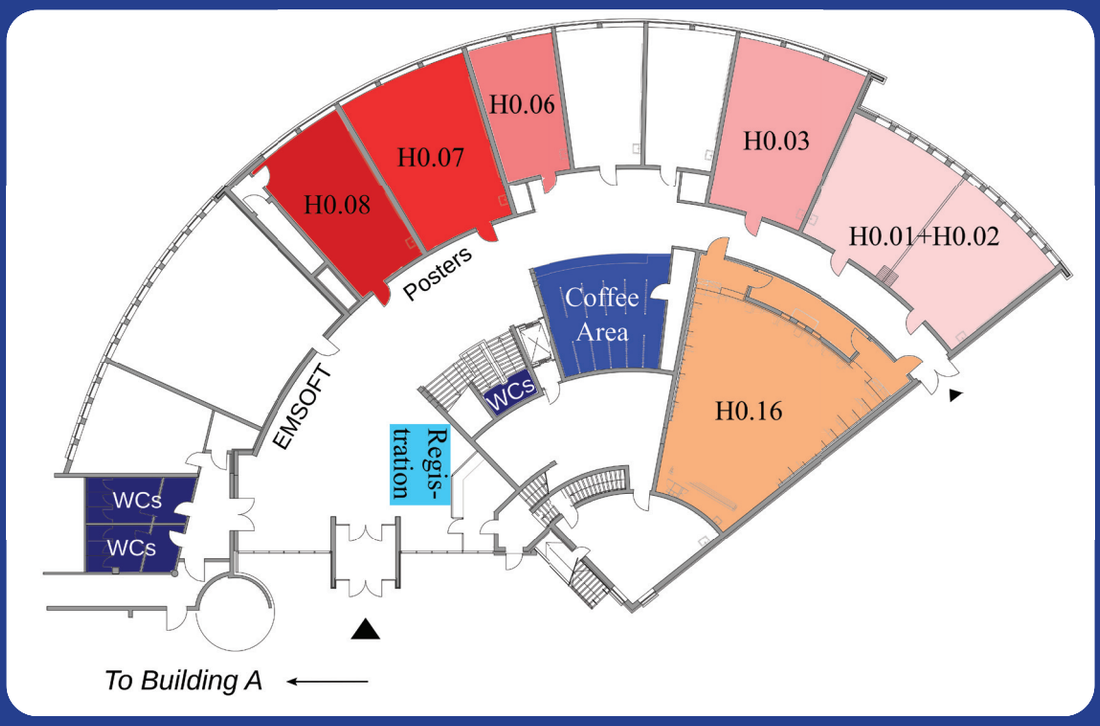
ESWEEK 2023 SCHEDULE AT-A-GLANCE

Friday, September 22

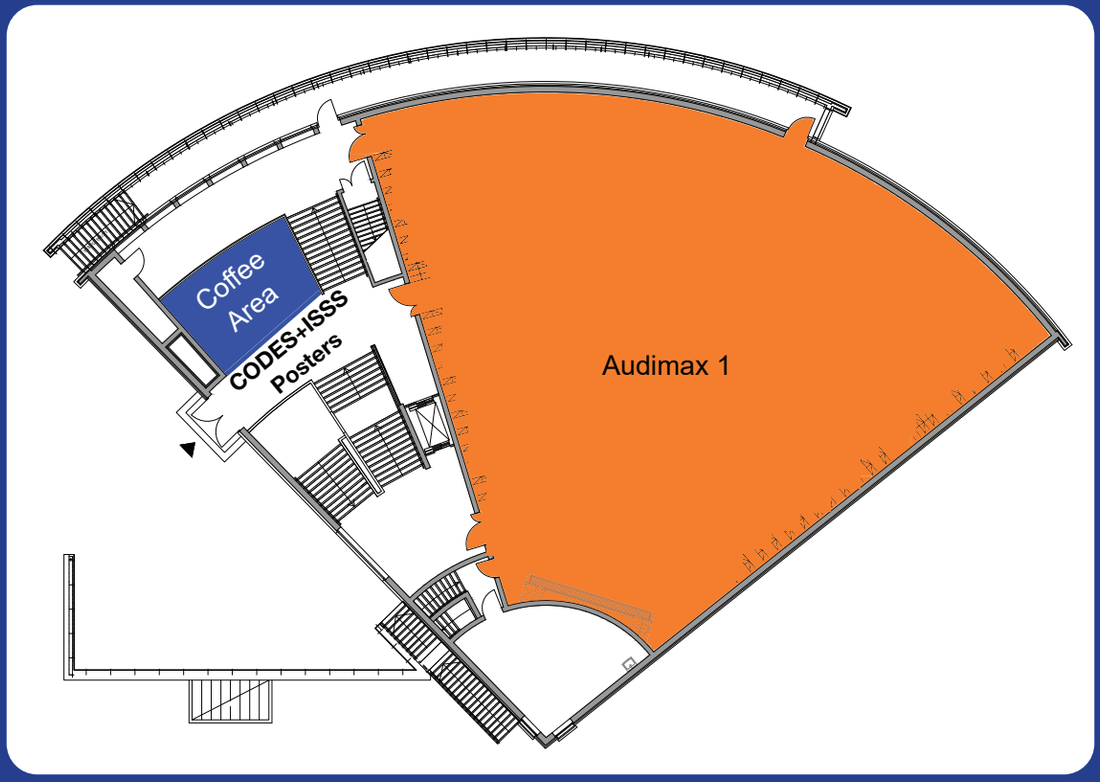
	H0.01 H0.02	H0.16
	MEMOCODE	**NOCS**
9:00 - 10:00	**Keynote 2:** Rolf Drechsler (Univ. Bremen)	**Keynote 2:** Diana Göhringer (TU Dresden)
10:00 - 10:30	Coffee Break	
10:30-12:30	**Technical Session 4: Hardware**	**Technical Session 4: NoC Modeling, Optimization, and Verification**
10:30-11:00	Symbolic Elaboration: Checking Generator Properties in Dynamic Hardware Description Languages	Fast Analysis using Finite Queuing Model for Multi-layer NoCs
11:00-11:30	Timestamp Peripherals for Precise Real-Time Programming	edAttack: Hardware Trojan Attack on On-Chip Packet Compression
11:30-12:00	Formally Verifying the Stall Invariant Property of Latency-Insensitive RTL Modules	Analytical Model for Performance Evaluation of Token-Passing Based WiNoCs
12:00-12:30	Formal Verification of Security Properties on RISC-V Processors	
12:30 - 13:30	Lunch Break	
13:30 - 15:00	**Technical Session 5: Models**	**Special Session on New Architectures and Techniques for Edge Intelligence**
13:30-14:00	Scalable Actor Networks with CAL	On Hardware-Aware Design and Optimization of Edge Intelligence
14:00-14:30	Constraint-Behavior Contracts: A Formalism for Specifying Physical Systems	Hardware/Software Co-Exploration for Hyperdimensional Computing on Network-on-Chip Architecture
14:30-15:00	Finding a Basis for Non-Sequential Endochronous Functions in Dataflow Process Networks	Automated Optical Accelerator Search: Expediting Green and Ubiquitous DNN-Powered Intelligence
15:00 - 15:30	Coffee Break	
15:30 - 17:00	**Closing Session**	**Closing Session and Panel**
15:30-16:00	MEMOCODE 2023 Best-Paper Award	NOCS 2023 Best-Paper Award
16:00-16:30	Review: MEMOCODE 2023 / Outlook: MEMOCODE 2024	Panel and Closing Remarks

ESWEEK 2023 VENUE AND AREA MAPS

H Ground Floor

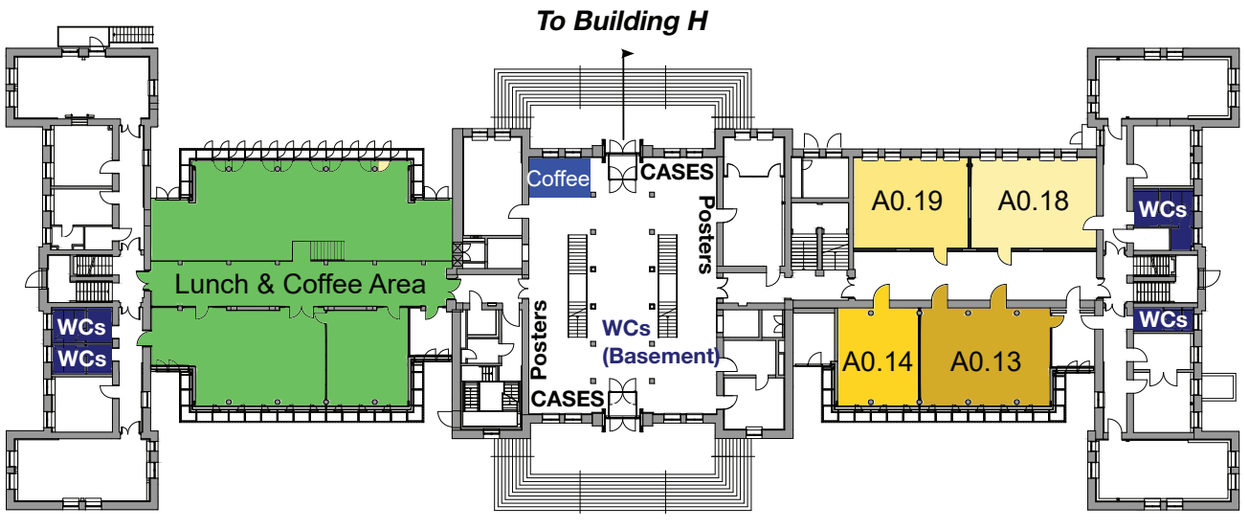


H First Floor

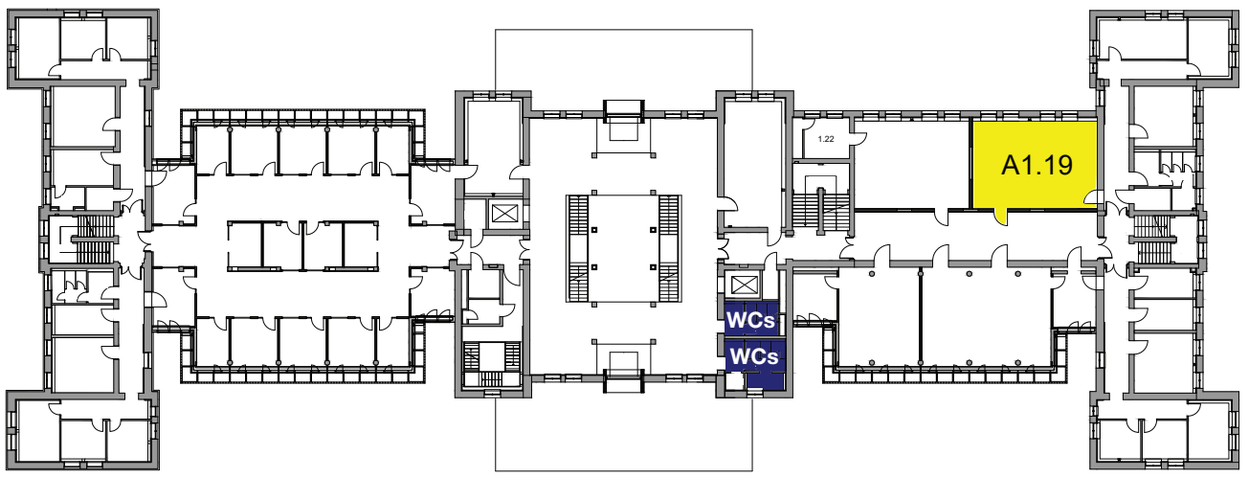


ESWEEK 2023 VENUE AND AREA MAPS

A Ground Floor

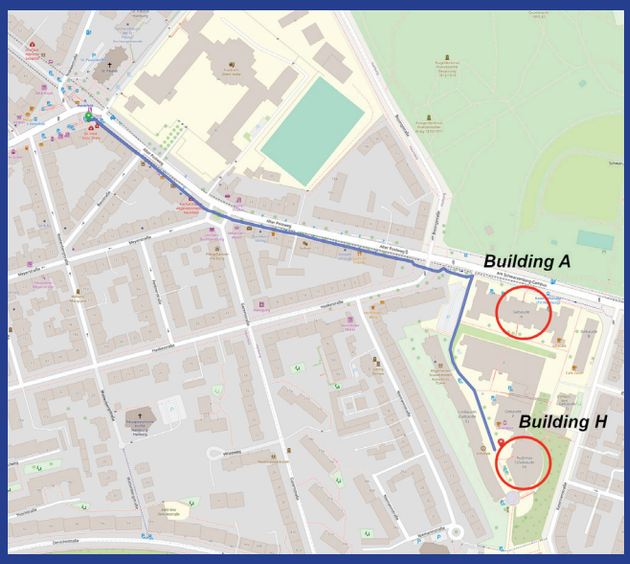


A First Floor

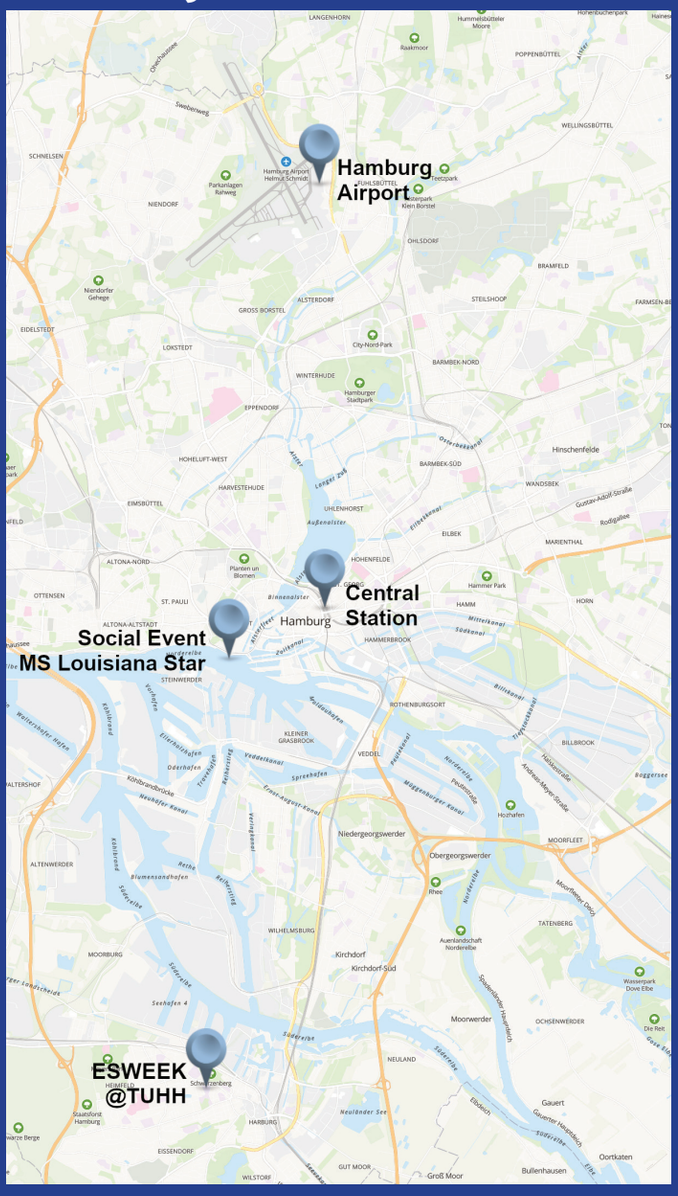


ESWEEK 2023 VENUE AND AREA MAPS

Directions to the Conference



Hamburg Points of Interest



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