Association for Computing Machinery

IEEE

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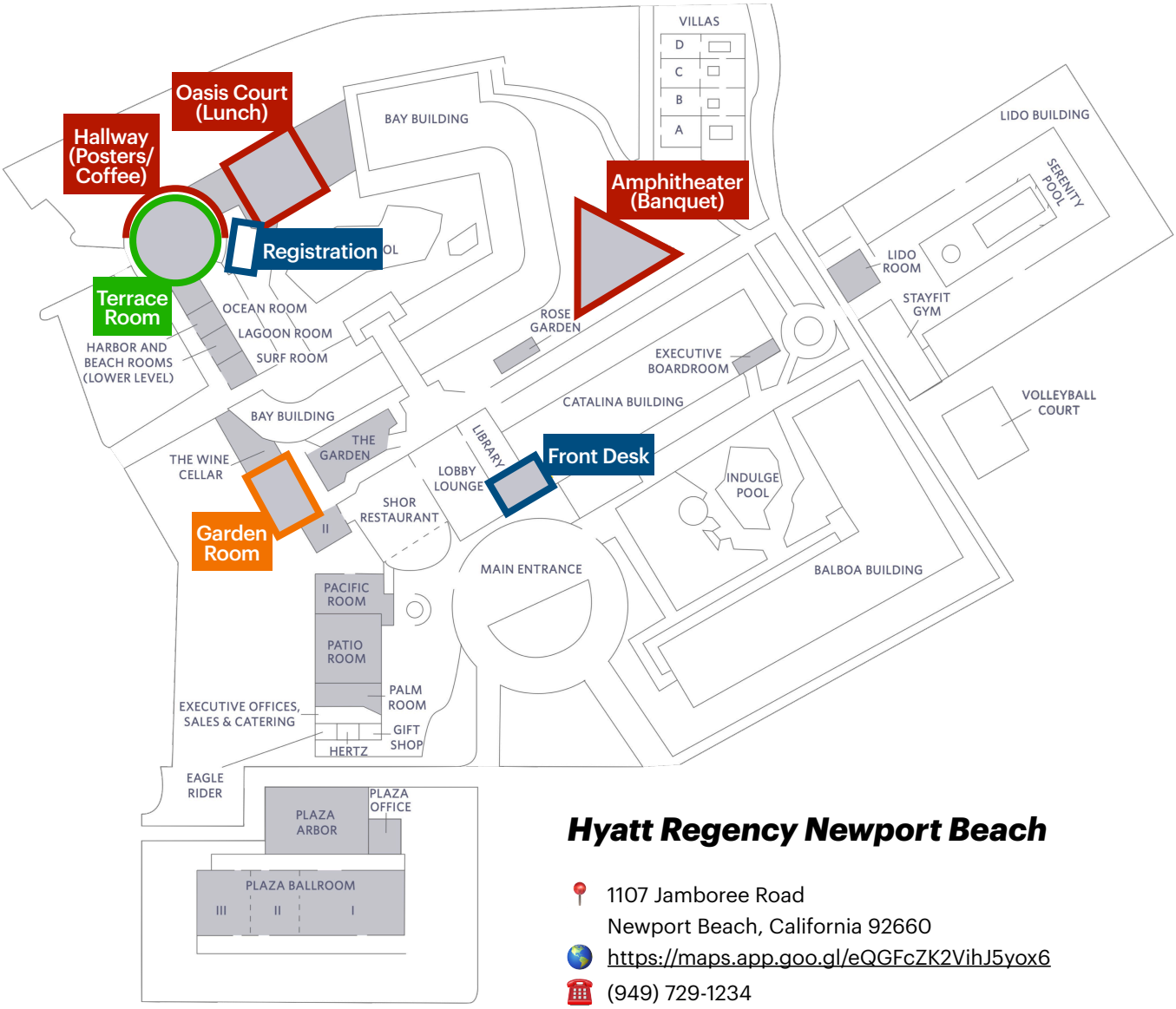

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PROGRAM OVERVIEW

T Terrace Room G Garden Room

Monday, August 5	7:30–8:00	**Registration**	
	8:00–8:30	**Welcome** T	
	8:30–9:30	**Keynote 1** T **Behzad Razavi, UCLA** *"Power Consumption Bounds in Wireline Transceivers"*	
	9:30–10:00	Coffee Break (Hallway)	
	10:00–11:40	**Session 1A** T *"Transformers and Natural Language Processing"*	**Session 1B** G *"Energy- and Carbon-efficient Machine Learning Techniques"*
	11:40–12:20	**Design Contest** T	
	12:20–13:40	**Lunch** (Oasis Court)	
	13:40–15:00	**Panel Discussion** T **Massoud Pedram, USC** *"Balancing Accuracy, Trust, and Efficiency in Edge AI: Is There a Sweet Spot?"*	
	15:00–16:40	**Session 2A** T *"Energy-Efficient Neural Networks via Algorithm-Hardware Co-optimization"*	**Session 2B** G *"Eye for the Detail: Bringing Security and Privacy to Nanoscale Systems"*
Tuesday, August 6	7:30–8:00	**Registration**	
	8:00–9:00	**Keynote 2** T **Vivek De, Intel** *"Attack-Resistant Energy-Efficient SoCs for Smart and Secure Cyberphysical Systems"*	
	9:00–9:30	Coffee Break (Hallway)	
	9:30–11:10	**Session 3A** T *"Emerging AI Accelerator Design"*	**Session 3B** G *"Advances in Power Modeling and Low Power Design Methods"*
	11:10–12:30	**Special Session** *"Low-power Heterogeneous Integration Platforms"*	
	12:30–13:40	**Lunch** (Oasis Court)	
	13:40–14:10	**Poster Pitch** T	
	14:10–15:10	**Poster Session** (Hallway, with coffee)	
	15:10–17:15	**Session 4A** T *"Next Generation Memories and Wearables"*	**Session 4B** G *"Optimizing Data Movement in Diverse Architectures: from VLIW to Optical Baseband Processors"*
	18:00–20:30	**Banquet** (Amphitheater)	
Wednesday, August 7	7:30–8:00	**Registration**	
	8:00–9:00	**Keynote 3** T **Kyomin Sohn, Samsung** *"Memory Solutions for On-device AI"*	
	9:30–9:30	Coffee Break (Hallway)	
	9:30–11:10	**Session 5** T *"Power Management and Energy Efficiency in AI Hardware Design"*	
	11:10–12:25	**Session 6** T *"Energy-Efficient Adaptive Internet-of-Things Systems"*	
	12:25–12:50	**Closing Remarks and Awards** T	

MONDAY TECHNICAL PROGRAM

8:30–9:30	**Keynote 1**
Terrace	Chair: Pascal A. Meinerzhagen, Intel
	Power Consumption Bounds in Wireline Transceivers Behzad Razavi, UCLA
10:00–11:40	**Session 1A: "Transformers and Natural Language Processing"**
Terrace	Chair: Dolly Sapra, University of Amsterdam
10:00–10:25	***A 28nm Scalable and Flexible Accelerator for Sparse Transformer Models (Best Paper Candidate)*** Yuan Liao, Jian Meng and Jae-sun Seo
10:25–10:50	***Hyft: A Reconfigurable Softmax Accelerator with Hybrid Numeric Format for both Training and Inference*** Tianhua Xia and Sai Qian Zhang
10:50–11:15	***PEANO-ViT: Power-Efficient Approximations of Non-Linearities in Vision Transformers*** Mohammad Erfan Sadeghi, Arash Fayyazi, Seyedarmin Azizi and Massoud Pedram
11:15–11:40	***Heterogeneous Memory Integration and Optimization for Energy-Efficient Multi-Task NLP Edge Inference*** Zirui Fu, Aleksandre Avaliani and Marco Donato
10:00–11:40	**Session 1B: "Energy- and Carbon-efficient Machine Learning Techniques"**
Garden	Chair: Kangmin Lee, Google
10:00–10:25	***LUTIN: Efficient Neural Network Inference with Table Lookup*** Shi-Zhe Lin, Yun-Chih Chen, Yuan-Hao Chang, Tei-Wei Kuo and Hsiang-Pang Li
10:25–10:50	***CLOVER: Carbon Optimization of Federated Learning over Heterogeneous Clients (Best Paper Candidate)*** Chanwoo Cho, Yonglak Son, Seongbin Park and Young Geun Kim
10:50–11:15	***Xyloni: Very Low Power Neural Network Accelerator for Intermittent Remote Visual Detection of Wildfire and Beyond*** Jeffrey Chen, Sang-Woo Jun, Aditi Mundra and Jonathan Ta
11:15–11:40	***EA²: Energy Efficient Adaptive Active Learning for Smart Wearables*** Hamidreza Alikhani Koshkak, Ziyu Wang, Anil Kanduri, Pasi Liljeberg, Amir M. Rahmani and Nikil Dutt
11:40–12:20	**Design Contest**
Terrace	Co-Chairs: Rajesh Kedia, IIT Hyderabad; Payam Heydari, University of California, Irvine
	Design and Applications of Low-Power RISC-V Multicore Processors with a Unified Lightweight FPU Jina Park, Kyeongwon Lee, Eunjin Choi, Hyunseok Kwak, Jae-Jin Lee, Kyuseung Han, Woojoo Lee and Massoud Pedram
	A Sub-1uJ/class SoC for Headset-Integrated Mind Imagery and Control in VR/MR Applications Zhiwei Zhong, Yijie Wei, Lance Go and Jie Gu

	eTag: An Energy-Neutral Ear Tag for Real-Time Body Temperature Monitoring of Dairy Cattle Hien Vu, Hanwook Chung, Christopher Choi and Younghyun Kim
	Viewer-Aware Low-Power Mobile Video System Destinie Diggs, William Oswald and Na Gong
13:40–15:00	**Panel Discussion**
Terrace	Organizer and Moderator: Massoud Pedram, University of Southern California
	Balancing Accuracy, Trust, and Efficiency in Edge AI: Is There a Sweet Spot? Yiran Chen, Duke University Hadi Esmaeilzadeh, University of California San Diego Kaushik Roy, Purdue University Amir Salek, Cereberus Capital Yanzhi Wang, Northeastern University
15:00–16:40	**Session 2A: "Energy-Efficient Neural Networks via Algorithm-Hardware Co-optimization"**
Terrace	Chair: Seungkyu Choi, Kyung Hee University
15:00–15:25	***SwiSS: Switchable Single-Sided Sparsity-based DNN Accelerators*** Shamik Kundu, Soumendu Kumar Ghosh, Arnab Raha and Deepak A. Mathaikutty
15:25–15:50	***PiQi: Partially Quantized DNN Inference on HMPSoCs*** Ehsan Aghapour, Yixian Shen, Dolly Sapra, Andy Pimentel and Anuj Pathania
15:50–16:15	***STARC: Crafting Low-Power Mixed-Signal Neuromorphic Processors by Bridging SNN Frameworks and Analog Designs*** Kyuseung Han, Hyunseok Kwak, Kwang-Il Oh, Sukho Lee, HyeongUk Jang, Jae-Jin Lee and Woojoo Lee
16:15–16:40	***Sparrow ECC: A Lightweight ECC Approach for HBM Refresh Reduction towards Energy-efficient DNN Inference (Best Paper Candidate)*** Hoseok Kim, Seung Hun Choi, Young-Ho Gong, Joonho Kong and Sung Woo Chung
15:00–16:15	**Session 2B: "Eye for the Detail: Bringing Security and Privacy to Nanoscale Systems"**
Garden	Chair: Marco Donato, Tufts University
15:00–15:25	***CIPUF: Towards On-chip Learnable Anomaly Detection with Compute-In-PUF Architecture*** Jianbo Liu, Boyang Cheng, Zephan M. Enciso, Steven Davis and Ningyuan Cao
15:25–15:50	***X-IMM: Mixed-Signal Iterative Montgomery Modular Multiplication*** Mehdi Kamal and Massoud Pedram
15:50–16:15	***Securing Deep Neural Networks on Edge from Membership Inference Attacks Using Trusted Execution Environments*** Cheng-Yun Yang, Gowri Ramshankar, Nicholas Eliopoulos, Purvish Jajal, Sudarshan Nambiar, Evan Miller, Xun Zhang, Dave (Jing) Tian, Shuo-Han Chen, Chiy-Ferng Perng and Yung-Hsiang Lu

TUESDAY TECHNICAL PROGRAM

8:00–9:00	**Keynote 2**
Terrace	Chair: Kapil Dev, Nvidia
	Attack-Resistant Energy-Efficient SoCs for Smart and Secure Cyberphysical Systems Vivek De, Intel
9:30–11:10	**Session 3A: "Emerging AI Accelerator Design"**
Terrace	Chair: Lei Jiang, Indiana University
9:30–9:55	***LowPASS: A Low Power PIM-based Accelerator with Speculative Scheme for SNNs*** Zongwu Wang, Fangxin Liu, Longyu Zhao, Shiyuan Huang and Li Jiang
9:55–10:20	***Systolic Array Acceleration of Spiking Neural Networks with Application-Independent Split-Time Temporal Coding*** Jeongjun Lee and Peng Li
10:20–10:45	***All You Need is Unary: End-to-End Unary Bit-stream Processing in Hyperdimensional Computing*** Mehran Shoushtari Moghadam, Sercan Aygun, Faeze S. Banitaba and M. Hassan Najafi
10:45–11:10	***An Energy-Efficient 3D Point Neural Network Accelerator with Fine-grained LiDAR-SoC Pipeline Structure (Best Paper Candidate)*** Bokyoung Seo, Jueun Jung, Donghyeon Han and Kyuho Jason Lee
9:30–11:10	**Session 3B: "Advances in Power Modeling and Low Power Design Methods"**
Garden	Chair: Amit Agarwal, Intel
9:30–9:55	***3D-Aware Low Power High-level Resource Binding and Co-Design*** Daniel Xing and Ankur Srivastava
9:55–10:20	***Unleashing Flexibility of ML-based Power Estimators Through Efficient Development Strategies (Best Paper Candidate)*** Yao Lu, Qijun Zhang and Zhiyao Xie
10:20–10:45	***3D IC Architecture Evaluation and Optimization with Digital Compute-in-Memory Designs*** Hyung Joon Byun, Udit Gupta and Jae-sun Seo
10:45–11:10	***Hetero-3D: PPA and Power Delivery Benefits of Heterogeneous 3D ICs with a Customized Physical Design Flow*** Lingjun Zhu, Jiawei Hu, Gauthaman Murali and Sung Kyu Lim
11:10–12:30	**Special Session: "Low-power Heterogeneous Integration Platforms"**
Terrace	Organizers: Vikram Jain, University of California, Berkeley; Marina Zapater, HES-SO Chairs: Vikram Jain, University of California, Berkeley; Jerald Yoo, Seoul National University
11:10–11:30	***Cross-layer Exploration of 2.5D Energy-Efficient Heterogeneous Chiplets Integration: From System Simulation to Open Hardware*** Anna Burdina, Gabriel Catel Torres, Davide Schiavone, Miguel Peón-Quirós, Giovanni Ansaloni, David Atienza and Marina Zapater
11:30–11:50	***Design Approach for Die-to-Die Interfaces to Enable Energy-Efficient Chiplet Systems*** Vikram Jain, Wei Tang, Zuoguo Wu, Viansa Schmulbach, Sophia Shao, Zhengya Zhang and Borivoje Nikolic
11:50–12:10	***Enabling Chiplet Integration: UCIe and the Future of Die-to-Die IO*** Zuoguo Wu

12:10–12:30	***An Open-source Generator for Lightweight UCIe D2D Interface to Enable Energy-Efficient Multi-Chiplet Systems at the Edge*** Vikram Jain
13:40–15:10 **Terrace and Hallway**	**Poster Pitch and Poster Session** Chair: Jerald Yoo, Seoul National University
	Poster Pitch in the Terrace Room, followed by Poster Session in the Hallway List of posters on p. 9
15:10–16:50 **Terrace**	**Session 4A: "Next Generation Memories and Wearables"** Chair: Sai Qian Zhang, New York University
15:10–15:35	***Coupled 7T 1C SRAM based In-memory Computing Architecture with Gain/Offset Error Auto-compensated SAR ADC*** Honggu Kim, Yerim An and Yong Shim
15:35–16:00	***Magnet Free Inductive Wireless Power and Data Transmission System For Fully Implantable Cochlear Implants (Best Paper Candidate)*** Mert Doğan, Ayşe Beyhan Türkyılmaz, Yasemin Engür and Haluk Külah
16:00–16:25	***Cooling the Chaos: Mitigating the Effect of Threshold Voltage Variation in Cryogenic CMOS Memories*** Rakshith Saligram, Amol Gaidhane, Yu Cao, Suman Datta and Arijit Raychowdhury
16:25–16:50	***STT-MRAM-based Near-Memory Computing Architecture with Read Scheme and Dataflow Co-Design for High-Throughput and Energy-Efficiency*** Yunho Jang, Yeseul Kim and Jongsun Park
15:10–17:15 **Garden**	**Session 4B: "Optimizing Data Movement in Diverse Architectures: from VLIW to Optical Baseband Processors"** Chair: Marco Donato, Tufts University
15:10–15:35	***GUMSO: Gating Unnecessary On-Chip Memory Slices for Power Optimization on GPUs*** Seunghyun Jin, Hyunwuk Lee and Won Woo Ro
15:35–16:00	***ReOVE: Restricted Out-of-Order Execution for Superscalar Processors with Vector Extension*** Masayuki Kimura and Ryota Shioya
16:00–16:25	***SPADES: A 0.54-GFLOPS/W Sparse Matrix Vector Multiplication Accelerator Featuring On-the-Fly GZIP Decompression for 3.36X Reduction in Off-Chip Data Movement*** Paul Xuanyuanliang Huang, Yannis P. Tsividis and Mingoo Seok
16:25–16:50	***ParaBase: A Configurable Parallel Baseband Processor for Ultra-High-Speed Inter-Satellite Optical Communications*** Seungkyu Choi, Huanshihong Deng, Kuan-Yu Chen, Yufan Yue, David Blaauw and Hun Seok Kim
16:50–17:15	***LOCo: LPDDR Optimization with Compression and IECC scheme for DNN Inference (Best Paper Candidate)*** Jae-Youn Hong, Sungkyu Kim, Je-Woo Jang and Joon-Sung Yang

WEDNESDAY TECHNICAL PROGRAM

8:00–9:00	**Keynote 3**
Terrace	Chair: Jerald Yoo, Seoul National University
	Memory Solutions for On-device AI Kyomin Sohn, Samsung
9:30–11:10	**Session 5: "Power Management and Energy Efficiency in AI Hardware Design"**
Terrace	Chair: Shamik Kundu, Intel
9:30–9:55	***Hardware Acceleration of Inference on Dynamic GNNs (Best Paper Candidate)*** Sudipta Mondal and Sachin S. Sapatnekar
9:55–10:20	***iSPADE: End-to-end Sparse Architecture for Dense DNN Acceleration via Inverted-bit Representation*** Dongjun Kim, Han Cho and Jongsun Park
10:20–10:45	***ePredictNet: Low Cost Error Prediction Neural Network*** Georgios Chatzitsompanis and Georgios Karakonstantis
10:45–11:10	***Energy Harvesting-Supported Efficient Low-Power ML Processing with Adaptive Checkpointing and Intermittent Computing*** Sanket Shukla and Sai Manoj Pudukotai Dinakarrao
11:10–12:25	**Session 6: "Energy-Efficient Adaptive Internet-of-Things Systems"**
Terrace	Chair: Younghyun Kim, Purdue University
11:10–11:35	***Rapid Hardware/Software Design Space Exploration for Efficient Intermittent Systems*** Youngbin Kim and Hyoseung Kim
11:35–12:00	***Statues: Energy-Efficient Video Object Detection on Edge Security Devices with Computational Skipping*** Yeonggeon Kim, Hyunmin Kim and Sungju Ryu
12:00–12:25	***Causes and Fixes of Unexpected Drone Shutoffs*** Choi Hojun, Chanyeok Choi and Youngmoon Lee

POSTERS

#	Tuesday 13:40–15:10 in Terrace and Hallway
1	***Energy Efficiency Through In-Sensor Computing: ADC-less Real-Time Sensing for Image Edge Detection*** Nirmoy Modak and Kaushik Roy
2	***FPIA: Field-Programmable Ising Arrays with In-Memory Computing*** George Hutchinson, Ethan J. Sifferman, Tinish Bhattacharya, Dongseok Kwon and Dmitri Strukov
3	***Cryogenic Operation of Computing-In-Memory based Spiking Neural Network*** Laith A. Shamieh, Weichun Wang, Shida Zhang, Rakshith Saligram, Amol Domaji Gaidhane, Yu Cao, Arijit Raychowdhury, Suman Datta and Saibal Mukhopadhyay
4	***EDeN: Enabling Low-Power CNN Inference on Edge Devices Using Prefetcher-assisted NVM Systems*** Jihoon Jang, Hyokeun Lee and Hyun Kim
5	***Triangle Counting in the Temporal Domain*** Caroline Ellis Hammond, Patricia Gonzalez-Guerrero, Meriam Gay Bautista and Nirmalendu Bikash Patra
6	***ML-INSIGHT: Machine Learning for Inrush Current Prediction and Power Switch Network Improvement*** Vikram Gopalakrishnan, Bing-Yue Wu and Vidya A. Chhabria
7	***HQ-DTM: A Hierarchical Q-learning Algorithm for Dynamic Thermal Management of Multi-core Processors*** Abir Ahsan Akib and Ankur Srivastava
8	***A Technology-Agnostic Method for Digital LDO Synthesis and Layout Automation*** Yaswanth Kumar Cherivirala and David Wentzloff
9	***PACT: Accurate Power Analysis and Carbon Emission Tracking for Sustainability*** Aditya Ukarande, Toygun Basaklar, Mingcong Cao and Umit Ogras
10	***DISHA: Low-Energy Sparse Transformer at Edge for Outdoor Navigation for the Visually Impaired Individuals*** Praveen Nagil and Sumit K. Mandal
11	***Content-based Power-saving Design for Augmented Reality Applications on Mobile Devices*** Ping-Han Chou, Shih-En Wei and Chun-Han Lin
12	***Energy-Efficient Frequency Selection Method for Bio-Signal Acquisition in AI/ML Wearables*** Hossein Taji, José Angel Miranda Calero, Miguel Peon Quiros and David Atienza Alonso
13	***VisionHD: Towards Efficient and Privacy-Preserved Hyperdimensional Computing for Image Data*** Fatemeh Asgarinejad, Justin Morris, Tajana Rosing and Baris Aksanli
14	***ComBoost: An Instruction Complexity Aware DTM Technique for Edge Devices*** Seung Hun Choi, Joonho Kong and Sung Woo Chung
15	***JointNF: Enhancing DNN Performance through Adaptive N:M Pruning across both Weight and Activation*** Sai Qian Zhang, Thierry Tambe, Gu-Yeon Wei and David Brooks
16	***HeTraX: Energy Efficient 3D Heterogeneous Manycore Architecture for Transformer Acceleration*** Pratyush Dhingra, Jana Doppa and Partha Pratim Pande
17	***Efficient Transformer Accelerator via Reconfiguration for Encoder and Decoder Dual Modes with Sparsity-Aware Data Mapping*** Chang Eun Song, Ashkan Moradifirouzabadi, Tajana Rosing and Mingu Kang

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1.1–1.2. Technologies and Circuits

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Deliang Fan, Arizona State University
Fady Abouzeid, ST Microelectronics
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Inhee Lee, University of Pittsburgh
Samantak Gangopadhyay, Meta
Alexandre Levisse, EPFL
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Srividhya Venkataraman, AMD
Ralf Brederlow, Technical University of Munich

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M. Hassan Najafi, University of Louisiana
Yang (Katie) Zhao, University of Minnesota
Marco Donato, Tufts University
Swagath Venkataramani, IBM

Track 2. CAD, Systems, and Software

2.1. CAD Tools and Methodologies

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Alberto Macii, Politecnico di Torino
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Sanghamitra Roy, Utah State University
Caaliph Andriamisaina, CEA-Leti
Yuko Hara-Azumi, Tokyo Institute of Technology
Aida Todri-Sanial, TU Eindhoven

2.2. Systems and Platforms

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Donghwa Shin, Soongsil University
Massimo Poncino, Politecnico di Torino
Pai Chou, National Cheng Kung University, Taiwan
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Mohammad Al Faruque, University of California, Irvine
Hussam Amrouch, Technical University of Munich
Taeyoung Kim, Intel
William Fornaciari, Politecnico di Milano
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Santhosh Rethinagiri, Infineon
Naehyuck Chang, KAIST
Rajesh Kedia, IIT, Hyderabad
Anuj Pathania, University of Amsterdam
Hyung Gyu Lee, Duksung University

2.3. Software and Applications

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Ittetsu Taniguchi, Osaka Unversity
Aporva Amarnath, IBM
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Wanli Chang, University of York
Geng Yuan, University of Georgia
Victor Kartsch, ETH Zurich
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Track 3. Crosscutting Topics

3.1. AI/ML Hardware, Compute-in-Memory (CIM) and Next-Generation Computing

Greg Chen (Track Co-Chair), Intel
Aatmesh Shrivastava (Track Co-Chair), Northeastern University
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Kanad Basu, University of Texas Dallas
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