Call for Papers

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ISLPED 2026

International Symposium on Low Power Electronics and Design

www.islped.org
Chicago, USA
August 5–7, 2026

Organizing Committee

General Co-Chairs
Younghyun Kim, Purdue Univ.
younghyun@purdue.edu
Srividhya Venkataraman, AMD
srividhya.venkataraman@amd.com

Program Co-Chairs
Mehdi Kamal, USC
mehdikamal@usc.edu
Aatmesh Shrivastava, Northeastern Univ.
aatmesh@northeastern.edu

Treasurer
Shahin Nazarian, USC
shahin.nazarian@usc.edu

Local Arrangement Co-Chairs
Jie Gu, Northwestern Univ.
jgu@northwestern.edu
Amit Trivedi, UIC
amitrt@uic.edu

Publications Co-Chairs
Xue Lin, Northeastern Univ.
xue.lin@northeastern.edu
Sudhanshu Khanna, TI
skhanna@ti.com

Registration Chair
Ganapati Bhat, WSU
ganapati.bhat@wsu.edu

Web Co-Chairs
Ganapati Bhat, WSU
ganapati.bhat@wsu.edu
Hein Vu, Purdue Univ.
hienvu@purdue.edu

Publicity Chair
Jinho Lee, Seoul National Univ.
leejinho@snu.ac.kr

Industry Liaison Chair
Adam Teman, Bar-Ilan Univ.
adam.teman@biu.ac.il

Women in Technology Co-Chairs
Priya Panda, Yale Univ.
priya.panda@yale.edu
Kathy Hoover, AMD
kathy.hoover@amd.com

Important Dates (Tentative)

Technical Papers (11:59 PST)
Abstract registration: March 2, 2026
Full paper: March 9, 2026

Invited Talk, Tutorial, and Special Session Proposals
April 6, 2026

Design Contest Applications
May 11, 2026

Notification of Acceptance
May 18, 2026

Camera-ready Submission
June 15, 2026

The **International Symposium on Low Power Electronics and Design (ISLPED)** is the premier venue for presenting innovative research in all aspects of low power electronics and design, including process technologies, analog/digital circuits, simulation and synthesis tools, AI/ML-enhanced EDA/CAD, system-level design, optimization, system software, and applications. Specific topics include, but are not limited to, the following three main tracks and sub-areas:

Track 1. Technology, Circuits, and Architecture

1.1. Technologies and Circuits
Low-power technologies for device, interconnect, logic, memory, 2.5/3D, cooling, harvesting, sensors, optical, printable, biomedical, battery, and alternative energy storage devices and technology enablers for non-Boolean and quantum/quantum-inspired compute models. Low-power circuits for logic, memory, reliability, yield, clocking, resiliency; low-power analog/mixed-signal circuits for wireless, RF, MEMS, ADC/DAC, I/O, PLLs/DLLs, DC-DC converters; energy-efficient circuits for emerging applications (e.g., neuromorphic, biomedical, in-vitro sensing, autonomous); circuits using emerging technologies; cryogenic circuits. DTCO for low power; combinatorial optimizers (Ising machine). AI/ML-based circuit optimization; circuit architecture for power-efficient AI applications.

1.2. Logic and Architecture
Low-power logic and microarchitecture for SoC designs, processor cores (compute, graphics, and other special purpose cores), cache, memory, arithmetic/signal processing, cryptography, variability, asynchronous design, and non-conventional computing. System technology co-optimization (STCO) for low power. AI/ML-assisted logic optimization and architecture exploration. Power efficient architecture for AI.

Track 2. EDA, Systems, and Software

2.1. CAD Tools and Methodologies
CAD tools, methodologies, and AI/ML-based approaches for low power and thermal-aware design (analog/digital). AI/ML for acceleration of IP block design convergence. Power estimation, optimization, reliability, and variation impact on power optimization at all levels of design abstraction: physical, circuit, gate, register transfer, behavior, and algorithm.

2.2. Systems and Platforms
Low-power, power-aware, and thermal-aware system design including data centers, SoCs, embedded systems, Internet-of-Things (IoT), wearable computing, body-area networks, wireless sensor networks, and system-level power implications due to reliability and variability. Applications of AI/ML-based solutions and brain-inspired computing to power-aware system and platform design.

2.3. Software and Applications
Energy-efficient, energy/thermal-aware software and application design, including scheduling and management, power optimization through HW/SW co-design, and emerging low-power AI/ML applications.

2.4. Hardware and System Security
Low-power hardware security primitives (PUF, TRNG, cryptographic/post-quantum cryptographic accelerators), nano-electronics security, supply chain security, IoT security and AI/ML security; confidential computing; energy-efficient approaches to system security.

Track 3. AI/ML, Quantum and Emerging Hardware

3.1. Analog, Mixed-Signal & Emerging AI Hardware
Analog and mixed-signal computing architectures for AI/ML including analog matrix multiplication, in-memory computing, and compute-in-memory techniques; emerging device technologies such as memristors, ReRAM, phase-change memory, and photonic computing; neuromorphic and brain-inspired computing systems including spiking neural networks; circuit design techniques for analog AI accelerators including ADC/DAC design, switched-capacitor networks, and noise-resilient architectures; EDA tools and methodologies for analog/mixed-signal AI systems including simulation, verification, and layout automation; process variation mitigation and robustness techniques for non-ideal analog computation.

3.2. Digital AI Hardware & Systems
Digital accelerator architectures including systolic arrays, dataflow architectures, and tensor processing units; ASIC, FPGA, and GPU-based implementations for AI/ML workloads; memory hierarchy design and optimization including high-bandwidth memory, scratchpads, and cache architectures; sparse computation and quantization hardware; RTL design, verification, and synthesis for AI accelerators; logic synthesis, place-and-route, timing closure, and power optimization for ML chips; system-level design including network-on-chip, interconnects, and multi-chip systems; compiler, runtime, and systems software for AI hardware; performance modeling, simulation, and design space exploration tools.

3.3. Quantum Computing and Emerging Computing Technologies
Quantum computing hardware platforms including superconducting qubits, trapped ions, and photonic systems; quantum algorithms, error correction, and fault tolerance; quantum circuit compilation and optimization; NISQ algorithms and hybrid quantum-classical systems; emerging post-CMOS paradigms including DNA computing, molecular computing, photonic computing, and probabilistic computing; neuromorphic and spin-based computing; EDA tools, programming frameworks, and benchmarking methodologies for quantum and emerging computing platforms.

Track 4. Industrial Design Track

This track solicits papers to reinforce interaction between the academic research community and industry. Industrial Design track papers have the same submission deadline as regular papers and should focus on similar topics but are expected to provide a complementary perspective to academic research by focusing on challenges, solutions, and lessons learnt while implementing industrial-scale designs.

Submissions (not published/accepted/under review by another journal, conference, symposium, or workshop) should be full-length papers of **up to 6 pages** (PDF format, double-column, US letter size, using the ACM Conference format available at https://www.acm.org/publications/proceedings-template) including all illustrations, tables, and an abstract of no more than 250 words, plus **an additional 1 page for references only**.

Accepted papers will be submitted to the IEEE Xplore Digital Library and the ACM Digital Library. ISLPED'26 will present three Best Paper Awards based on the ratings of reviewers and a panel of judges. Selected papers will be invited to submit an extended version for publication in the **IEEE Transactions on Very Large Scale Integration.**

There will be several invited talks by industry and academic thought leaders on key issues in low-power electronics and design. The Symposium may also include embedded tutorials to provide attendees with the necessary background to follow recent research results, as well as panel discussions on future directions in low-power electronics and design. Proposals for invited talks, embedded tutorials, and panels should be sent by email to the ISLPED'26 Technical Program Co-Chairs by the deadline listed on the left. Participants interested in exhibiting at the Symposium should contact the General Chairs by May 1, 2026.

Important update on ACMs new open access publishing model for 2026 ACM Conferences!

Starting January 1, 2026, ACM will fully transition to Open Access. All ACM publications, including those from ACM-sponsored conferences, will be 100% Open Access. Authors will have two primary options for publishing Open Access articles with ACM: the ACM Open institutional model or by paying Article Processing Charges (APCs). With over 2,600 institutions already part of ACM Open, the majority of ACM-sponsored conference papers will not require APCs from authors or conferences (currently, around 76%).
Authors from institutions not participating in ACM Open will need to pay an APC to publish their papers, unless they qualify for a financial waiver. To find out whether an APC applies to your article, please consult the list of participating institutions in ACM Open and review the https://www.acm.org/publications/policies/policy-on-discretionary-open-access-apc-waivers. Keep in mind that waivers are rare and are granted based on specific criteria set by ACM.
Understanding that this change could present financial challenges, ACM has approved a temporary subsidy for 2026 to ease the transition and allow more time for institutions to join ACM Open. The subsidy will offer:

- $250 APC for ACM/SIG members
- $350 for non-members

This represents a 65% discount, funded directly by ACM. Authors are encouraged to help advocate for their institutions to join ACM Open during this transition period.
This temporary subsidized pricing will apply to all conferences scheduled for 2026.

Additional Notes to Authors

- **Author Responsibility:** Submitters must obtain consent from all co-authors for the submission of the manuscript and ensure that their correct author information is provided by the abstract registration deadline.
- **Changes to Author List:** After abstract registration, changes to the author list—including additions, removals, or reordering of authors—are not permitted. However, the corresponding author may be changed up until the camera-ready submission deadline.
- **Anonymity Requirements:** Submissions must be anonymous. Authors' names or affiliations must not appear in the manuscript or the registered abstract. References to the authors' prior work must be cited in the third person, and phrases such as "omitted for blind review" are not allowed in the reference section. PDF metadata must not include any author information. Submissions that fail to meet these blind-review requirements will be automatically rejected without review.
- **Formatting Guidelines:** The manuscript must not exceed 6 pages (excluding references) and must follow the ACM style template without significant modification. This includes maintaining the specified margins, line spacing, and using a double-column format in 9- or 10-point font. Submissions must be in PDF format, readable, and adhere to the template requirements.
- **Additional Reference Page:** References may be included within the 6-page limit or on one additional page. Inclusion of any non-reference content on the reference page will result in desk rejection. The manuscript and reference page must be combined into a single PDF file.
- **Submission Consistency:** The content and length of the submitted manuscript must not be significantly different to those of the camera-ready version, if accepted.
- **Use of Generative AI Software:** Authors may use generative AI software tools to prepare the paper. However, you must disclose their use in either the acknowledgements section of the work or elsewhere in the work prominently. Please refer to the following FAQ webpage for more information about the ACM publication policies: https://www.acm.org/publications/policies/frequently-asked-questions